



Cite as

Nano-Micro Lett.
(2026) 18:216

Received: 13 October 2025
Accepted: 27 December 2025
© The Author(s) 2026

Dipole-Driven Charge Trapping in Monolayer Janus MoSSe for Ultrathin Nonvolatile Memory Devices

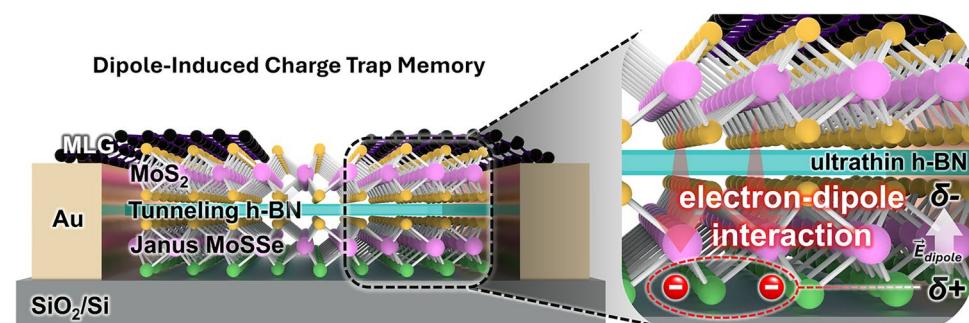
Eun Bee Ko¹, Junho Sung², Seon Yeon Choi¹, Yasir Hassan³, Jeong-Ju Bae³,
Jongseok Kim³, Hyun You Kim³, Eunho Lee², Min Sup Choi³ , Hyun Ho Kim^{1,4}

HIGHLIGHTS

- Janus MoSSe-based floating-gate memory exhibits ultrafast charge-trapping dynamics and stable charge retention exceeding 10^8 s under low-voltage operation.
- The intrinsic out-of-plane dipole moment in Janus MoSSe effectively suppresses leakage current and enlarges the memory window, even with ultrathin h-BN tunneling layers.
- The proposed all-van der Waals heterostructure provides a scalable platform for high-speed, energy-efficient, and reliable nonvolatile memory applications.

ABSTRACT The continued scaling of flash memory technologies faces challenges such as limited operation speed, poor data retention, and interface defects inherent to conventional three-dimensional architectures. Two-dimensional (2D) materials, with van der Waals interfaces and atomic-scale thickness, offer a promising pathway to

overcome these limitations by enabling efficient charge modulation while minimizing surface defects. In this work, a nonvolatile 2D flash memory device is developed employing monolayer Janus MoSSe as the charge-trapping layer and hexagonal boron nitride (h-BN) as an ultrathin tunneling barrier. The intrinsic structural asymmetry of Janus MoSSe induces a strong vertical dipole moment, resulting in enhanced charge trapping, deeper energy barriers, and directional polarization compared with symmetric 2D materials. Consequently, the devices exhibit outstanding retention times exceeding 10^4 s, endurance beyond 10^4 program/erase cycles, and large memory window ratios ($\Delta V/V_{G,\max}$ of 50%–70% for 10 and 6 nm h-BN, respectively), with charge-trapping rates up to $8.96 \times 10^{14} \text{ cm}^{-2} \text{ s}^{-1}$. In addition, Janus MoSSe-based devices show synaptic characteristics under electrical pulses and perform recognition simulations in artificial neural networks. These findings establish a design paradigm for 2D memory devices, enabling ultrathin, flexible, and energy-efficient nonvolatile memories.



KEYWORDS Janus TMDs; Nonvolatile memory; Floating-gate; 2D materials; Synaptic device

Min Sup Choi, goodcms@cnu.ac.kr; Hyun Ho Kim, kimhh@gist.ac.kr

¹ School of Materials Science and Engineering, Kumoh National Institute of Technology, Gumi 39177, Republic of Korea

² Department of Chemical and Biomolecular Engineering, Seoul National University of Science and Technology, Seoul 01811, Republic of Korea

³ Department of Materials Science and Engineering, Chungnam National University, Daejeon 34134, Republic of Korea

⁴ School of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangju 61005, Republic of Korea

1 Introduction

Nonvolatile flash memory devices are key components in the advancement of next-generation electronics, particularly for ultrafast, highly stable, and high-density data storage in the modern semiconductor industry [1]. As digital infrastructure increasingly demands energy-efficient and scalable memory technologies for applications such as flexible electronics [2], wearables, neuromorphic computing [3], and the Internet of Things, the development of high-performance memory devices becomes even more critical [4, 5]. However, conventional 3D flash memory architectures are facing scaling bottlenecks, including low operation speeds, short data retention, limited endurance, and poor interface quality, which stem from issues such as surface dangling bonds, interface roughness, and inefficient charge tunneling [6, 7]. To overcome these limitations, two-dimensional (2D) materials have emerged as highly promising candidates. Their atomic thinness, the absence of surface dangling bonds, and clean van der Waals (vdW) interfaces enable precise electrostatic control, efficient charge modulation, and defect-minimized device behavior [8–11]. These advantages have driven significant research into 2D-material-based memory, logic, and optoelectronic devices [12].

Among the critical design parameters for 2D flash memory devices, the tunneling barrier and the charge trapping layer are decisive factors that govern memory window, retention time, and endurance. Dielectric materials such as hexagonal boron nitride (h-BN) [13], aluminum oxide (Al_2O_3) [14], and hafnium oxide (HfO_2) [15] have been widely employed as tunneling barriers owing to their large bandgap and chemical stability. In parallel, 2D materials including MoS_2 [13], graphene [16], and WSe_2 [9] have been explored as charge trapping layers because of their atomic thinness and compatibility with vdW heterostructures. Despite these advances, their performance is often limited by symmetric charge distribution and shallow trapping centers, which result in reduced charge retention, accelerated leakage, and relatively narrow memory windows [17]. These intrinsic drawbacks underscore the urgent need for alternative charge-trapping materials that can provide deeper and more stable trap states, enhanced polarity, and improved electrostatic control.

In this work, we introduce the use of monolayer Janus MoSSe as a charge trapping material in a 2D flash memory device. Janus MoSSe, a unique transition metal

dichalcogenide (TMD), possesses a built-in vertical dipole due to its structural asymmetry, with sulfur (S) atoms on one side and selenium (Se) on the other side [18, 19]. This internal electric field not only enhances charge trapping and retention but also introduces directional charge polarization, which is unavailable in conventional symmetric 2D TMDs. The fabricated 2D memory device with Janus MoSSe charge trapping layer exhibits exceptional performance, long-term stability of 10^4 s, endurance up to 10^4 program/erase cycles, high memory window, $\Delta V/V_{G,\max}$ ratio of 50% (10 nm h-BN) and 70% (6 nm h-BN) at a charge trapping rate of $2.97 \times 10^{14} \text{ cm}^{-2} \text{ s}^{-1}$ for the 10-nm-thick h-BN device and $8.96 \times 10^{14} \text{ cm}^{-2} \text{ s}^{-1}$ for the 6-nm-thick h-BN device, compared to previously reported 2D-material-based flash memories. Janus MoSSe with intrinsic dipole enables deeper and stable trapping states and higher energy barriers, resulting in superior charge retention and reduced charge leakage. Asymmetric charge transport arising from the alignment between the intrinsic dipole and the external gate electric field leads to a preferential, one-sided expansion of the memory window. The combination of h-BN and Janus MoSSe ensures both efficient tunneling and robust charge confinement, a balance rarely achieved in prior systems. Finally, the fabricated device successfully achieved synaptic weight updates such as paired-pulse facilitation (PPF), long-term plasticity (LTP), and long-term potentiation/depression (LTP/D). We also achieved high accuracy in artificial neural network (ANN)-based simulations reflecting the obtained device characteristics. This study establishes a new design paradigm for 2D flash memory devices by leveraging the asymmetric dipolar nature of Janus MoSSe, achieving unprecedented memory performance metrics in a simple and scalable architecture. These findings pave the way for next-generation, ultrathin, high-performance non-volatile memories with applications in AI hardware, flexible electronics, and low-power logic circuits.

2 Experimental Section

2.1 Device Fabrication and Characterization

2.1.1 Stamp Preparation

The poly(bisphenol A carbonate) (PC) film was prepared by dissolving it in chloroform at a concentration of 0.15 g mL^{-1} .

The solution was drop-cast onto a glass slide to form a film, which was subsequently dried. The dried PC film was then attached to a polydimethylsiloxane (PDMS, PF-40/17-X4, Gel-Pak) block, and the PDMS block was fixed onto a glass slide to serve as a stamp.

2.1.2 Device Fabrication

The heterostructured memory devices were fabricated inside a nitrogen-atmosphere glovebox ($P_{O_2}, P_{H_2O} < 0.1$ ppm) equipped with a custom-built microscope/transfer system. The process began by picking up graphene, which served as the contact electrode. Subsequently, the channel layer (MoS_2) was aligned and picked up, followed by sequential pickup of the tunneling layer (h-BN) and the floating-gate layer (Janus MoSSe). Detailed procedures for the pickup process have been described previously [20]. The assembled stack was then transferred onto a pre-patterned Ti/Au (3/30 nm) electrode deposited on a p-type Si substrate with a 285-nm SiO_2 layer (Silicon Technology Co.). After transfer, the supporting PC film was removed using chloroform.

2.1.3 Characterization

Micro-Raman spectroscopy (UniRAM, UniNanoTech) with a 532-nm excitation laser was employed to characterize $MoSe_2$ and Janus MoSSe grown on SiO_2/Si substrates. Electrical measurements were performed at room temperature in ambient conditions using two DC source meters (Keithley 2450) with needle-type probes. The thickness of 2D materials, including Janus MoSSe, was measured in tapping mode using atomic force microscopy (FX40, Park Systems).

2.2 Simulation and Computational Methods

2.2.1 Simulation Parameter

The dynamic range was obtained from the on/off ratio of the LTP/D curves, while NS_{eff} was defined as the number of valid conductance states exceeding a noise level, set at 0.5% of $G_{max} - G_{min}$. NL values were calculated using the following equations [21, 22]:

$$G_{LTP} = B \left(1 - e^{-\left(\frac{P}{A_p} \right)} \right) + G_{min} \quad (1)$$

$$G_{LTD} = -B \left(1 - e^{\left(\frac{P - P_{max}}{A_D} \right)} \right) + G_{max} \quad (2)$$

$$B = (G_{max} - G_{min}) / (1 - e^{-\frac{P_{max}}{A_{p,D}}}) \quad (3)$$

where G represents the conductance value in the LTP/D curve, P is the number of applied pulses, and A denotes a fitting parameter governing nonlinearity in EPSC modulation.

2.2.2 ANN-based Simulation Details

The ANN simulations were performed on a Linux system utilizing the open-access software MLP + NeuroSimV3.0 based on a multilayer perceptron structure. The ANN was designed with an input layer comprising 784 neurons (corresponding to 28×28 pixels), a hidden layer of 100 neurons, and an output layer of 10 neurons representing digits 0–9. The 60,000 images used in training were processed in batches of 8,000 images per epoch with a batch size of 64, and the size of the weights was standardized for maximum = 1 and minimum = -1. To consider the characteristics of Janus MoSSe-based devices, we used device characteristic values such as nonlinearity (NL) dynamic range, gate/drain voltage, pulse number, and cycle-to-cycle (C2C) and device-to-device (D2D) variation. C2C variation was defined as the percentage term of the conductance range defined as $G_{max} - G_{min}$. D2D variation was calculated as the standard deviation of NL values between different devices, and the larger of the LTP and LTD regions was reflected in the simulation to be conservative.

2.2.3 CNN-based Simulation Details

CNN simulations were performed on a Linux system using the open-source program DNN + NeuroSimV2.1 to evaluate the classification accuracy on CIFAR-10 data. For the computation, we adopted a VGG-8 structure consisting of six convolutional/pooling layers and two fully connected layers. During the training and inference process, the images were converted into feature maps (FMs) consisting of the input signals (V) and weights (W) convolved with the current

signal (I). The generated FMs were transformed through ReLU activation functions and scaled down and emphasized through max-pooling in the 2nd, 4th, and 6th layers. Learning and inference were then successfully performed through the fully connected layers. To reflect the characteristics of Janus MoSSe-based devices in these computations, device parameters were applied as in the ANN-based simulations.

2.2.4 Density Functional Theory Calculations

All spin-polarized DFT calculations were performed using the Vienna ab initio simulation package (VASP) code and the Perdew–Burke–Ernzerhof (PBE) functional [23–25]. The projector augmented wave method describes the interaction between the ionic core and valence electrons [24]. The DFT + U scheme [26], with $U_{\text{eff}} = 4 \text{ eV}$ [27], was applied to the Mo ions to treat the localized Mo-d orbitals appropriately. Valence electron wave functions were expanded on a plane-wave basis up to an energy cutoff of 400 eV. The first Brillouin zone was sampled at the Γ -point for initial geometry optimizations and expanded to a $6 \times 6 \times 1$ grid for further electronic analyses. Convergence criteria for electronic structure and atomic geometries were 10^{-4} eV and 0.05 eV \AA^{-1} , respectively. A Gaussian smearing function with a finite temperature width of 0.01 eV was employed to enhance the convergence of states near the Fermi level. The initial MoS_2 motif was adopted from our previous study [28]. To virtually reproduce the overall geometry of the Janus MoSSe floating-gate memory device, we combined two $4 \times 4 \text{ MoS}_2$ layers (top and bottom) and a h-BN interfacial layer. The h-BN- MoS_2 interlayer spacing was initially set to the literature-reported vdW distance [29] and optimized. The bottom-most S atoms in the bottom MoS_2 layer were substituted with Se to construct the final Janus MoSSe-h-BN- MoS_2 model structure (Fig. S2). The vacuum layer between the Janus MoSSe-h-BN- MoS_2 triple layers was set to 10 Å.

3 Results and Discussion

3.1 Structural Asymmetry and Charge–Dipole Interaction Mechanism of Janus MoSSe

A novel memory device structure that exploits the built-in dipole moment of Janus TMDs is investigated. Janus TMDs

possess an asymmetric atomic configuration, in which the top and bottom chalcogen layers are composed of distinct atomic species. This out-of-plane asymmetry gives rise to a permanent electric dipole, leading to strong charge–dipole interactions that significantly influence the charge trapping behavior in memory devices. The unique atomic configuration and structural characteristics of Janus TMDs are illustrated in Fig. 1a. To realize this structure experimentally, MoSe_2 was grown using a conventional atmospheric pressure chemical vapor deposition (APCVD) method (Fig. S1a) [30]. Specifically, single-crystalline MoSe_2 nanosheets were synthesized in an APCVD reactor under an Ar/H_2 atmosphere, using MoO_3 and Se powder as precursors. The as-grown MoSe_2 nanosheets were then converted into Janus MoSSe nanosheets by applying a previously reported plasma-induced sulfurization method (Fig. S1b) [31]. In this process, the top Se atoms were replaced with S under an Ar/H_2 plasma environment, thereby forming a Janus structure with S on the top layer and Se on the bottom layer. The synthesized Janus MoSSe was examined by optical microscopy (OM) and confirmed to exist as a monolayer by atomic force microscopy (AFM) (Fig. S1c, d). Raman spectroscopy was performed to examine the structural characteristics of the Janus MoSSe. As shown in Fig. S1e, the Raman spectrum of Janus MoSSe exhibits clear peak shifts compared to that of MoSe_2 , indicating successful Janus conversion. Raman mapping analysis further reveals a uniform intensity distribution across the entire Janus MoSSe flake, confirming good spatial uniformity without noticeable degradation (Fig. S1f). In addition, the photoluminescence (PL) spectrum shows a well-defined emission peak, suggesting favorable optical quality of the synthesized Janus MoSSe (Fig. S1g) [30]. Figure S1h further presents the transfer characteristics of a Janus MoSSe transistor, confirming its n-type semiconducting behavior.

Following the verification of the optical characteristics of the synthesized Janus MoSSe, we performed theoretical analysis of the interaction between the built-in dipole moment and electrons in a vdW heterostructure-based floating-gate memory device incorporating Janus TMDs as the floating gate through density functional theory (DFT) calculation. To confirm that the Janus MoSSe captures and localizes excess electrons, we added a total of five electrons (corresponding to 0.5% of total electrons) to the neutral $\text{MoS}_2/\text{h-BN}/\text{Janus MoSSe}$ heterostructure. We separately present the density of states of each MoS_2 and

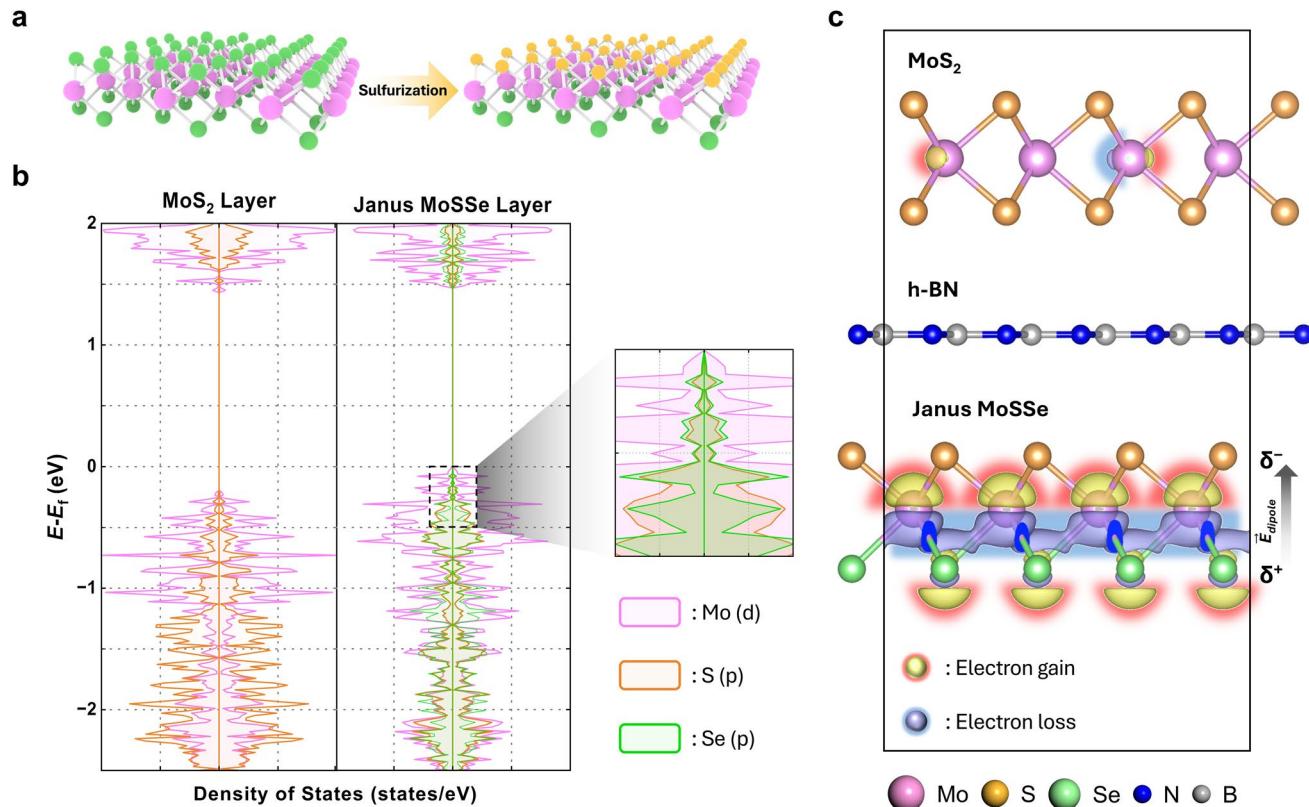


Fig. 1 **a** Schematic illustration of the sulfuration process converting MoSe₂ into Janus MoSSe by substituting the top Se atoms with S atoms. **b** DFT-calculated density of states (DOS) of each MoS₂ and Janus MoSSe layer, showing a pronounced contribution of Se p-orbitals near the Fermi level in the Janus structure upon electron injection. **c** Charge density difference map of the MoS₂/h-BN/Janus MoSSe heterostructure, where yellow and blue regions represent the area where electrons are localized or depleted

Janus MoSSe layer (Fig. 1b) and the corresponding charge density difference map (Fig. 1c), illustrating the orbitals at which the injected electrons are localized. The DOS confirms that the Se *p*-orbitals contribute to the occupied electron states near the Fermi level (Fig. 1b), indicating that Se atoms strongly attract electrons. The charge density difference map of MoS₂/h-BN/Janus MoSSe heterostructure confirms that injected electrons are primarily localized at Se atoms (yellow area). Furthermore, electron gain (yellow area) and loss (blue area) pairs are accordingly formed around Mo atoms upon electron localization at the Se atoms. The electronic behavior of the MoS₂/h-BN/Janus MoSSe heterostructure demonstrates that the intrinsic polarity of the Janus structure drives electron localization at Se sites, accompanied by a rearrangement of Mo states. Moreover, the comparison in Fig. S2 between MoS₂/h-BN/MoS₂ and MoS₂/h-BN/Janus MoSSe heterostructures reveals distinct variations in interface distance,

bond length, and bond angle, confirming that the structural asymmetry introduced by the Janus layer directly affects both the electronic distribution and the structural characteristics of the heterostructure.

To further elucidate the role of dipole orientation, we additionally performed theoretical calculations on an inverted Janus MoSSe structure, in which the Se-terminated side faces upward (Fig. S3). For the original Janus MoSSe configuration, the injected electrons are primarily stabilized within the Janus MoSSe layer, consistent with effective the charge confinement by the built-in dipole field. In contrast, for the inverted Janus MoSSe structure, the calculated charge density difference map reveals noticeable electron accumulation in the MoS₂ channel region as well. This redistribution of injected charges toward the channel can be interpreted as a leakage-like behavior, which is expected to degrade charge-trapping stability. These theoretical results indicate that the orientation of the intrinsic dipole plays a

critical role in determining charge redistribution and confinement. When combined with the experimentally observed polarity-dependent electrical characteristics, the enhanced ΔV_{th} and memory window only under the positive sweep (electron injection) for Janus MoSSe the results consistently support the interpretation that the built-in dipole in Janus MoSSe actively contributes to the charge-trapping behavior. Although a direct experimental visualization of the dipole field is beyond the scope of this work, the qualitative agreement between experiment and theory provides a coherent physical picture for the dipole-assisted charge-trapping mechanism in Janus MoSSe.

3.2 Device Architecture and Memory Characteristics of Janus MoSSe-Based Floating-Gate Memories

Figure 2a presents a schematic of the 2D flash memory device, in which multilayer graphene (MLG)/MoS₂/h-BN/Janus MoSSe are vertically stacked on a p-Si/SiO₂ substrate. Here, p-Si and SiO₂ function as the control gate and blocking layer, respectively, while Janus MoSSe serves as the floating gate, h-BN as the tunneling layer, MoS₂ as the channel, and MLG as the source/drain electrodes. Graphene-TMD heterostructures have been utilized for high-performance electronic devices with atomically clean interfaces [32]. As shown in the band diagram of Fig. 2b, the built-in out-of-plane dipole in Janus MoSSe generates an internal electric field (E_{dipole}). Consequently, when electrons are trapped under an applied gate voltage, they are expected to localize near the Se atoms, as evidenced by prior DFT calculation. This localization of electrons, governed not only by the electric field (E_{ext}) from the gate voltage but also by the inherent dipole field, enables more effective tunneling and charge storage, thereby enlarging the memory window (ΔV) and prolonging charge retention. In contrast, the Janus MoSSe-based structure proposed in this study is fundamentally distinct from previously reported 2D NVMs in that it does not rely on defect-mediated mechanisms [33] or structural phase transitions [34], but instead directly exploits the intrinsic out-of-plane built-in dipole of Janus MoSSe in the charge storage and injection processes. This inherent dipole asymmetrically modulates the tunneling barrier depending on its alignment with the external gate field, thereby facilitating electron injection while suppressing charge release. As a result, enhanced charge-trapping characteristics can be

achieved without artificial trap engineering. Such dipole-engineered operation represents a previously unreported mechanism in 2D material-based memory devices and demonstrates the feasibility of a flash memory architecture that directly employs Janus MoSSe as a floating gate.

Figure 2c shows the OM image of an actual fabricated device. Other 2D materials employed in this study, excluding Janus MoSSe, were mechanically exfoliated and subsequently stacked to form vdW heterostructures (see Methods and Fig. S4 for detailed fabrication steps). Figure 2d shows the transfer characteristics measured under different gate-voltage sweep conditions. The drain voltage (V_{DS}) was fixed at 0.1 V, while the control gate voltage (V_G) was swept between ± 80 V. A pronounced hysteresis window was observed, confirming the nonvolatile memory operation of Janus MoSSe floating-gate devices. For comparison, a control device employing MoSe₂ as the floating gate, with an otherwise identical structure, exhibited a relatively small hysteresis window under the same measurement conditions (Fig. 2e). As shown in Fig. 2f, the memory window of both devices increased proportionally with the maximum swept gate voltage ($V_{G,max}$). At $V_{G,max} = \pm 80$ V, Janus MoSSe-based device exhibited a memory window of $\Delta V = 79.4$ V, approximately 1.5 times larger than that of the MoSe₂-based device ($\Delta V = 52.8$ V). Compared with the MoSe₂-based device, the Janus MoSSe-based device exhibits a more pronounced increase in the memory window in the positive gate-voltage direction. This behavior can be attributed to the intrinsic structural asymmetry of Janus MoSSe and its associated dipole moment, which enhances charge trapping when aligned with the applied positive gate electric field. This enhancement arises from the inherent structural asymmetry and built-in dipole moment of Janus MoSSe, which promote more efficient charge trapping compared to symmetric TMDs.

To evaluate memory reliability, endurance and retention characteristics of Janus MoSSe-based devices were investigated. As shown in Fig. 2g, the drain current (I_D) was monitored at $V_G = 0$ V over time with program/erase pulses of ± 80 V for 1 s duration. Both program and erase states remained highly stable up to 10^4 s, and extrapolation predicts data retention exceeding 10 years. Retention measurements at elevated temperatures of 85 and 100 °C further confirm the thermal stability of the stored charges, showing negligible variation in both programmed and erased states (Fig. S5a). Furthermore, endurance cycling

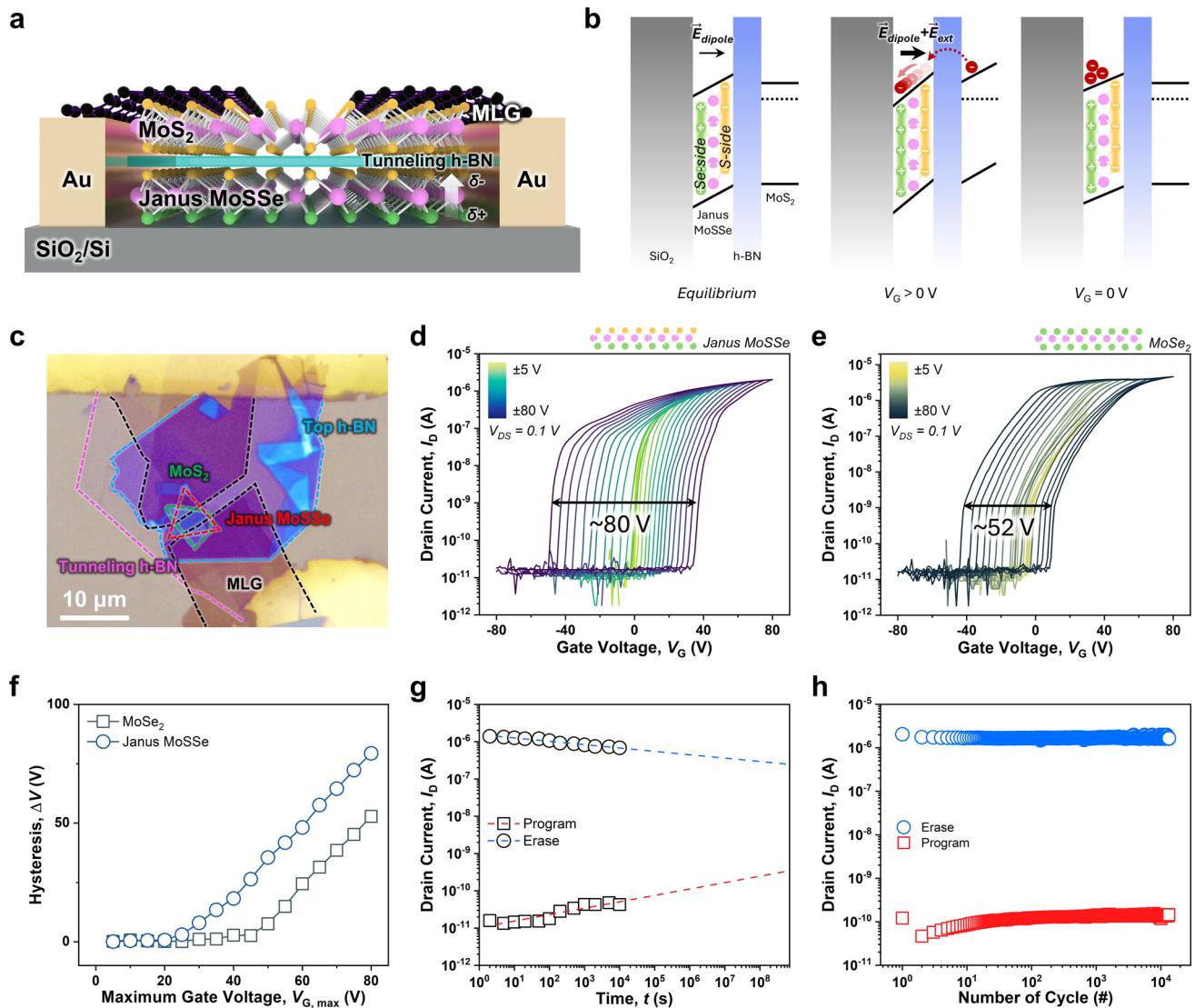


Fig. 2 Janus MoSSe floating-gate memory device with 10 nm h-BN as the tunneling layer. **a** Schematic illustration of the vdW heterostructure device. **b** Schematic energy band diagram. **c** OM image of the fabricated device. Transfer curves of **d** Janus MoSSe and **e** MoSe_2 devices measured under gate sweeps ($\pm 5 \sim 80 \text{ V}$) at $V_{DS} = 0.1 \text{ V}$. **f** ΔV of Janus MoSSe and MoSe_2 devices as a function of maximum gate voltage. **g** Retention performance measured at $V_G = 0 \text{ V}$ with a pulse of $\pm 80 \text{ V}$, 1 s gate pulses and $V_{DS} = 0.1 \text{ V}$. **h** Endurance characteristics under repeated program/erase cycling up to 10^4 cycles

tests (Fig. 2h), performed using $\pm 80 \text{ V}$ program/erase pulses with a pulse width of 30 ms, demonstrated reliable operation up to $\sim 10^4$ program/erase cycles without significant degradation, confirming the robust memory characteristics of Janus MoSSe floating-gate devices. To examine faster operation, the device was also tested using shorter program/erase pulses down to 500 ns, under which clear and stable program and erase states were still observed (Fig. S5b).

The data depicted in Fig. 2 correspond to devices integrating an h-BN tunneling layer with a thickness of approximately 10 nm. Decreasing the h-BN layer thickness enhances electron tunneling probability, thereby facilitating faster program/erase operations and enabling the development of high-speed memory devices. Nonetheless, excessively thinning the h-BN layer results in increased leakage current, which adversely affects retention performance. Conversely, increasing the thickness of h-BN suppresses electron tunneling, leading to slower program/erase responses and a

narrower memory window, yet effectively diminishes leakage current, thus promoting improved long-term data retention and device reliability [17, 35]. Owing to these inherent trade-offs, prior studies have established that an h-BN layer thickness of approximately 10 nm achieves an optimal compromise between tunneling efficiency and retention properties [7, 35, 36]. To further validate this proposed optimum and enhance device performance, the thickness of the tunneling layer was systematically varied from 4 to 16 nm to compare their transfer characteristics (Fig. S6). Notably, the Janus MoSSe floating-gate memory exhibited the largest memory window at an h-BN thickness of about 6 nm (Fig. S7a). This shift in the optimal tunneling layer thickness can be attributed to the presence of the intrinsic out-of-plane dipole in Janus MoSSe. Unlike conventional floating-gate systems, the built-in dipole field in Janus MoSSe enhances electron injection while simultaneously suppressing charge leakage, even when the tunneling barrier is relatively thin. As a result, efficient charge trapping can be maintained at a reduced h-BN thickness of ~6 nm, leading to a larger memory window compared to thicker tunneling layers. This behavior highlights the distinct role of the Janus dipole in modifying the conventional trade-off between tunneling efficiency and retention performance. In addition, a weak current suppression is observed in the transfer curves of the Janus MoSSe device with a 6-nm h-BN tunneling layer. This behavior is attributed to dipole-induced electrostatic modulation of the channel by trapped charges in the Janus MoSSe floating gate, rather than charge leakage, as the memory window continues to increase beyond this region.

Furthermore, devices incorporating bilayer Janus MoSSe as the floating gate were also fabricated and evaluated. The bilayer device exhibits a slightly increased memory window compared to the monolayer-based device; however, the overall performance characteristics remain similar (Fig. S8).

3.3 Effect of h-BN Tunneling Layer Thickness on Charge-Trapping and Retention Behavior

In light of these results, Fig. 3 presents a comparative analysis of memory performance between a 6-nm- and 10-nm-thick h-BN tunneling layers. For comparison, the thickness of each of the h-BNs used was verified via AFM (Fig. S9). This approach is predicated on the hypothesis that the

intrinsic built-in dipole moment of Janus MoSSe may mitigate the retention loss generally associated with thinner tunneling layers. Figure 3a–c and 3d–f show the program/erase characteristics of Janus MoSSe floating-gate memory devices employing 10-nm- and 6-nm-thick h-BN tunneling layers, respectively, under varying pulse widths. Figure 3a, d shows forward transfer curves from –40 to 40 V after applying an erasing voltage of –80 V with different widths. In contrast, Fig. 3b, e shows backward curves after applying a programming voltage of +80 V with different widths. Each transfer curve was obtained after an independently applied program or erase pulse followed by a gate-voltage sweep, ensuring that all data represent independent measurements without cumulative or history effects. Prolonged pulse durations promote threshold voltage (V_{th}) modulation due to increased charge trapping, resulting in an enlarged memory window. Figure 3c, f further illustrates V_{th} shifts and corresponding charge trapping rates as a function of programming pulse width, as described by the following equations:

$$\frac{dN_{trap}}{dt} = \frac{C_{total}}{e} \cdot \frac{dV_G}{dt}, dV_G/dt \approx \frac{\Delta V_{th}}{\Delta t} \quad (4)$$

Here, C_{total} represents the sum of the capacitances of SiO_2 , h-BN, and Janus MoSSe, e is the elementary charge, Δt is the pulse width, and ΔV_{th} denotes the threshold voltage shift induced by programming pulse [13]. Using this approach, the calculated charge trapping rate for the 6-nm-thick h-BN device was $8.96 \times 10^{14} \text{ cm}^{-2} \text{ s}^{-1}$ at pulse width of 100 μs , which is approximately three times higher than that of the 10-nm-thick h-BN device ($2.97 \times 10^{14} \text{ cm}^{-2} \text{ s}^{-1}$). Notably, the Janus MoSSe-based device maintained sufficient threshold voltage shifts and high trapping rates even under short pulse widths, with these characteristics more pronounced at the 6-nm h-BN thickness. This demonstrates that reducing the h-BN thickness significantly increases electron tunneling probability, thereby enhancing program/erase speeds, and also suggests that the built-in dipole structure of Janus MoSSe enables efficient charge trapping and storage even with thin dielectric layers.

In contrast, MoSe_2 -based devices exhibited a reduced memory window as the h-BN thickness decreased (Fig. S7). The charge trapping rate for the 10-nm-thick h-BN device was $2.12 \times 10^{14} \text{ cm}^{-2} \text{ s}^{-1}$, which decreased to $3.34 \times 10^{13} \text{ cm}^{-2} \text{ s}^{-1}$ at 6 nm, representing an approximately 6.4-fold reduction (Fig. S10). These results

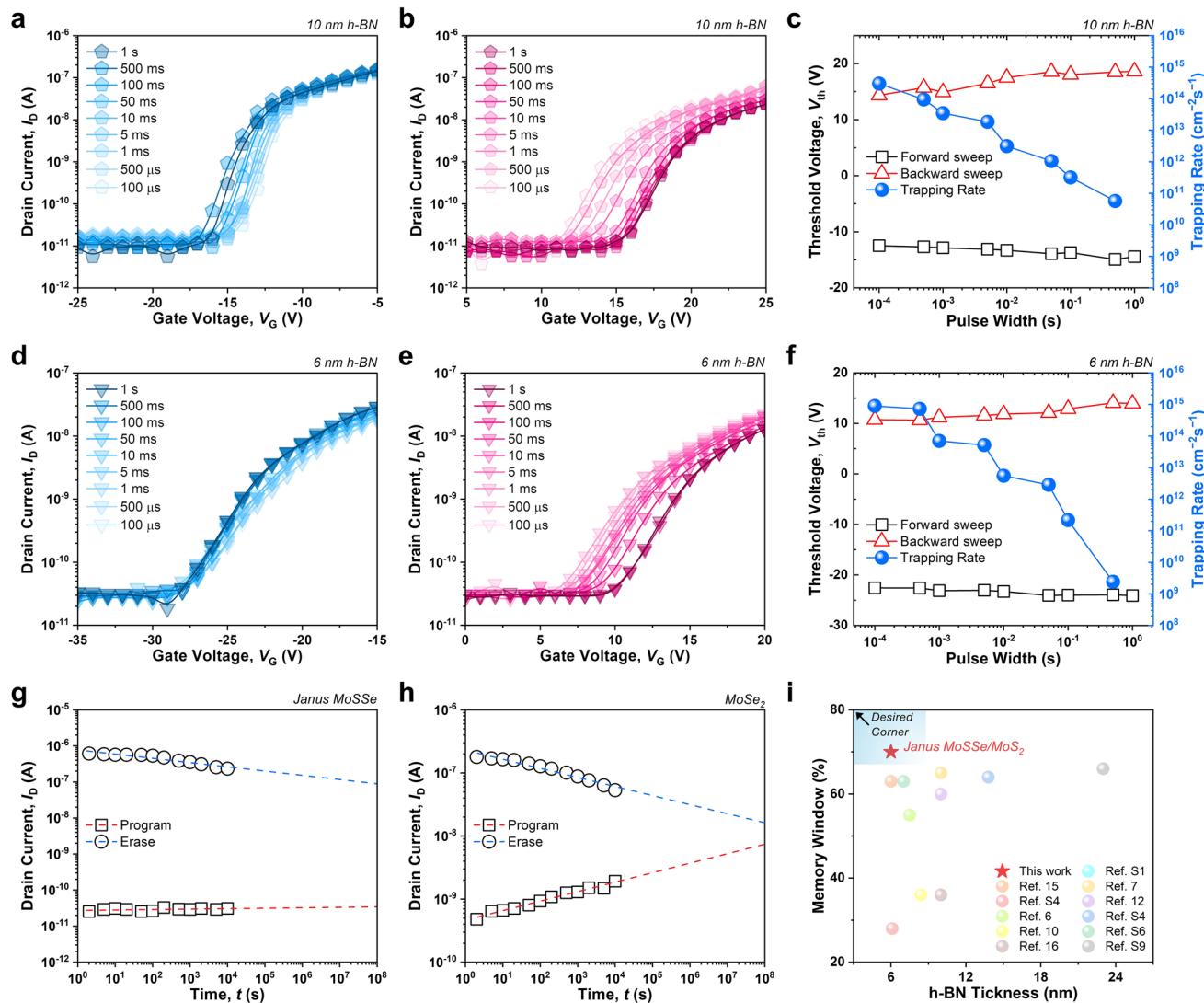


Fig. 3 Memory characteristics of Janus MoSSe and MoSe₂ floating-gate memory devices with different h-BN tunneling layer thicknesses. **a–c** Janus MoSSe memory devices with a 10-nm h-BN tunneling layer, and **d–f** devices with a 6-nm h-BN tunneling layer. **a, d** Transfer characteristics measured after applying -80 V gate pulses with pulse widths from 1 s to 100 μ s, read by a -40 to 40 V gate sweep; **b, e** Transfer characteristics under $+80$ V gate pulses measured under identical read conditions; **c, f** Corresponding threshold voltage shift (ΔV_{th}) and calculated charge trapping rate. Retention performance of **g** Janus MoSSe and **h** MoSe₂ memory devices with 6-nm h-BN tunneling layer, measured at $V_G=0$ V with a pulse of ± 80 V (1 s gate pulses) and $V_{DS}=0.1$ V. **i** Memory window as a function of h-BN thickness for this work and previously reported 2D floating-gate memory devices

suggest that thinner h-BN layers detrimentally affect charge trapping efficiency in MoSe₂-based devices. At 6-nm h-BN thickness, the charge trapping rate in the MoSe₂ device was approximately 26.8 times slower than that of the Janus MoSSe device. This degradation is mainly attributed to the absence of a built-in dipole moment in MoSe₂, which limits its ability to suppress leakage current and stabilize charge storage under ultrathin tunneling layer conditions. This highlights the critical role of the

intrinsic built-in dipole moment in Janus TMDs, which significantly enhances charge trapping performance with ultrathin dielectric thicknesses.

Figure 3g, h compares the retention characteristics of Janus MoSSe and MoSe₂ floating-gate memory devices using a 6-nm h-BN tunneling layer. Janus MoSSe exhibited long-term stability with a gradual decrease in I_D , retaining 76.5% of its initial on/off ratio (from 4.38 to 3.35 decades after 10 years) similar to the behavior observed at

10 nm h-BN. In contrast, MoSe_2 -based devices showed a rapid current decrease, with the on/off ratio decreasing from 2.57 to 0.19 decades, corresponding to only 7.4% retention. This contrast demonstrates that the built-in dipole in the Janus structure provides deeper and more stable charge trapping sites due to localized electrons in Se atoms, thereby enhancing retention performance.

Figure 3i compares the memory window as a function of h-BN thickness between this work and previously reported 2D floating-gate memory devices. We found that our Janus MoSSe floating-gate devices achieved a record memory window at a tunneling barrier thickness of 6 nm. Compared with Janus MoSSe devices, MoSe_2 floating-gate devices exhibited an overall smaller memory window, with a particularly pronounced decline at the 6 nm thickness (Fig. S7). The extracted memory window values and device characteristics are summarized in Table S1 for quantitative comparison. These results highlight that the structural asymmetry and inherent dipole moment in Janus materials are key factors that overcome the limitations of conventional TMD-based memory devices and enable excellent memory performance even with ultrathin dielectric layers.

Our findings are currently limited to the practical application of large-area Janus MoSSe due to manual device fabrication. Nevertheless, it is expected to be sufficiently scalable through the currently reported techniques and studies. In particular, for Janus MoSSe, large-scale synthesis is expected to be possible through the currently developed wafer-scale single crystal growth method of TMD and room-temperature plasma substitution [37]. Furthermore, the h-BN used as a tunneling layer in this study is sufficiently replaceable with ALD-depositable Al_2O_3 and HfO_2 [38]. In this respect, our Janus MoSSe memory shows inherent scalability potential.

3.4 Synaptic Plasticity and Neuromorphic Computing Performance of Janus MoSSe Memory Devices

To evaluate the potential of Janus MoSSe-based memory devices as neuromorphic systems, we implement the excitatory postsynaptic potential (EPSP) behavior of biological signaling (Fig. 4a). To mimic biological behavior in a memory device, we observed fluctuations in excitatory postsynaptic current (EPSC) induced by applied pulses. To realize short-term synaptic plasticity (STP), we examined the paired-pulse facilitation (PPF) property, an enhanced

response following two consecutive stimuli [39]. We found that the PPF index (A_2/A_1), defined as the ratio of the EPSC (A_2) to the second pulse to the EPSC (A_1) to the first pulse, decreased as the pulse interval increased (Fig. 4b). This decreasing trend was fitted with a quadratic exponential function [40–42]:

$$PPF = C_0 + C_1 \exp(-\Delta t/\tau_1) + C_2 \exp(-\Delta t/\tau_2) \quad (5)$$

where C_0 is the constant, and C and τ represent the facilitation magnitude and the relaxation time constants, respectively (τ_1 : slow phase, τ_2 : rapid phase). The fitting results yielded τ values on the order of several hundred milliseconds, consistent with previously reported PPF behavior [43–45]. In addition, for long-term plasticity (LTP) with continuous stimulation, we applied 10 pulses ($t_{\text{pulse}} = t_{\text{interval}} = 60$ ms) (Fig. 4c). The Janus MoSSe device showed a rapid increase in EPSCs upon pulse application, with current retention behavior of at least 87% for 240 s duration. These characteristics were also tunable via pulse width and number, and these results demonstrate that the EPSC response can be tuned compositely to enable multi-state realization (Fig. S11), which is a key requirement for in-memory computing using 2D-material-based memtransistor arrays [46].

In neuromorphic computing simulations, LTP/D is considered to be an important factor for neural network systems as it implements synaptic weight updates [47]. To investigate the LTP/D characteristics of the Janus MoSSe-based device, we applied 32 potentiation pulses (-60 V) and 32 depression pulses ($+30$ V) successively (Fig. 4d). To assess stability under repeated operation, we monitored the EPSC responses during 100 LTP/D cycles consisting of a total of 6400 pulses. Throughout the cycles, the device exhibited stable operation with consistently reproducible weighted potentiation and inhibition (Fig. S12). Finally, we extracted values of device characteristics such as NL and dynamic range (G_{\max}/G_{\min}) from the LTP/D curves to perform simulations in an artificial neural network (see details in the Experimental Section). These properties remained stable over 100 cycles without significant degradation (Fig. S13). In addition to stability over cycles, LTP/D curves extracted from five different devices confirmed that there was no significant variation between devices (Fig. S14). Based on the obtained characteristics of Janus MoSSe devices, we performed training and inference on a multilayer perceptron (MLP)-based ANN for MNIST digit recognition (Fig. 4e). Figure 4f shows the parallelizable array circuit design used

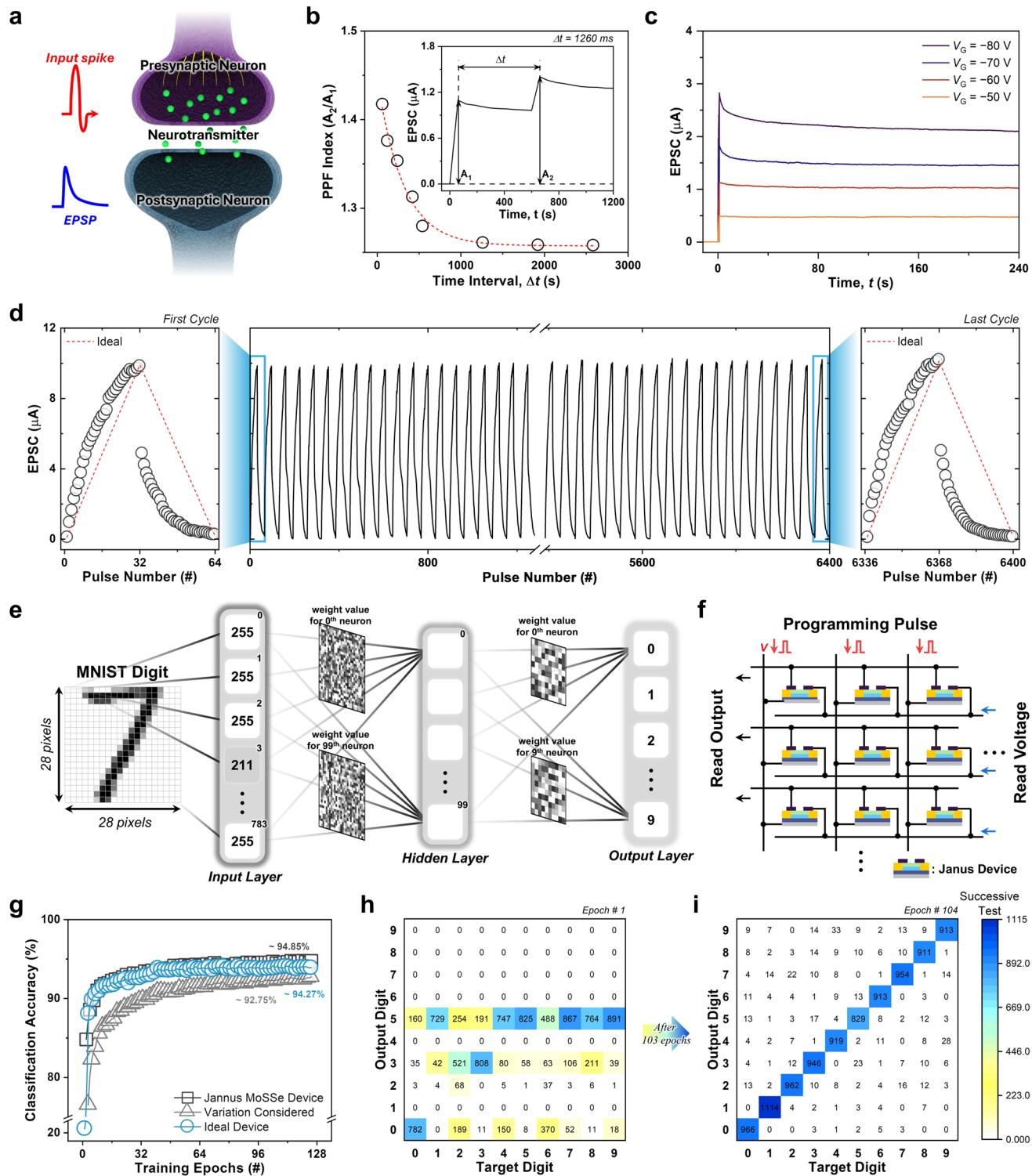


Fig. 4 Neuromorphic computing applications of Janus MoSSe-based devices. **a** A unit of signal transmission in the biological nervous system consisting of pre- and post-synaptic neurons and neurotransmitters. **b** The variation over time interval (Δt) of the PPF index (A_2/A_1), defined as the ratio of the response to the first pulse (A_1) to the response to the second pulse (A_2) for a pair of consecutively applied pulses. Inset: EPSC response when the Δt is 1260 ms. **c** Long-term plasticity characteristics following the application of 10 pulses with different amplitudes ($V_{pulse} = -80, -70, -60$, and -50 V). **d** LTP/D curve of a Janus MoSSe device under 64 pulses and LTP/D characteristics change over 100 cycles. **e** Multilayer perceptron consisting of input, hidden, and output layers for ANN operations. **f** Schematic diagram of synaptic array with Janus MoSSe devices and circuits. **g** Recognition accuracy of Ideal device and Janus MoSSe device and D2D and C2C variation considered Janus MoSSe devices over 125 epochs. Confusion matrix for recognition accuracy of MNIST digits at **h** at 1 epoch and **i** 104 epochs

to implement the ANN weight connections in the simulation. Values such as NL , dynamic range, and variation were applied to the computation to reflect the characteristics of the device. Simulation results show that the recognition accuracy is close to the ideal device at 94.27% (Fig. 4g). Recognition simulations based on the characteristics of Janus MoSSe memory showed that it can reliably perform computations with 92.75% accuracy, even considering variations between devices and cycles. The confusion matrix for MNIST digit recognition showed random recognition in the first epoch, but as the learning progressed, it showed a clear diagonal pattern and achieved successful learning (Fig. 4h). Janus MoSSe memory was also able to perform stable simulations on convolutional neural networks (CNNs), which are based on more complex and higher-order computations (Fig. S15). Taken together, these results confirm that the Janus MoSSe-based parallel processing system can reliably support not only simple pattern recognition but also advanced computational tasks, highlighting its strong potential for neuromorphic computing.

4 Conclusions

In conclusion, this study successfully demonstrates a 2D nonvolatile flash memory device utilizing Janus MoSSe as the floating gate. The intrinsic dipole moment originating from the structural asymmetry of Janus MoSSe was identified, through both theoretical calculations and experimental validation, to play a pivotal role in charge trapping and storage. This built-in asymmetry induces electron localization and strong charge–dipole interactions, resulting in superior device performance with a wide memory window, excellent retention, endurance exceeding 10^4 program/erase cycles, and rapid charge-trapping dynamics. Optimization of the h-BN tunneling thickness enabled a favorable balance between charge injection efficiency and retention, even at reduced thicknesses, evidencing that the intrinsic polarity of Janus MoSSe fundamentally enhances memory operation. Furthermore, Janus MoSSe-based devices exhibited promising neuromorphic functionalities applicable to neural network learning and recognition. These findings provide valuable guidelines for designing ultrafast and reliable nonvolatile memories based on Janus TMDs. They further highlight the potential of these materials in

next-generation flexible electronics and artificial intelligence hardware.

Acknowledgements This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (RS-2025-23323229, RS-2022-NR072277, RS-2021-NR060128, 2022M3H4A1A04085325, RS-2025-24534310). It was also supported by the K-CHIPS program (RS-2024-00405798) funded by the Ministry of Trade, Industry and Energy (MOTIE) and by the Korea Evaluation Institute of Industrial Technology (KEIT) grant funded by the Korean government (MOTIE) (RS-2024-00420534).

Author Contributions Eun Bee Ko and Junho Sung contributed equally to this work. Eun Bee Ko and Junho Sung contributed to investigation and original draft writing. Seon Yeon Choi was involved in investigation, Yasir Hassan contributed to original draft writing, and Jeong-Jo Bae and Jongseok Kim were involved in formal analysis. Hyun You Kim and Eunho Lee contributed to review writing. Min Sup Choi and Hyun Ho Kim were involved in conceptualization, review, and supervision.

Declarations

Conflict of interest The authors declare no interest conflict. They have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by/4.0/>.

Supplementary Information The online version contains supplementary material available at <https://doi.org/10.1007/s40820-026-02078-y>.

References

1. J. Shi, Z. Liu, J. Wei, A. Azam, C.-H. Lin et al., Revolutionizing nonvolatile memory: advances and future prospects of 2D floating-gate technology. *ACS Nano* **19**(24), 21905–21926 (2025). <https://doi.org/10.1021/acsnano.5c02740>
2. M. Naqi, B. Kim, S.-W. Kim, S. Kim, Pulsed gate switching of MoS₂ field-effect transistor based on flexible polyimide

substrate for ultrasonic detectors. *Adv. Funct. Mater.* **31**(7), 2007389 (2021). <https://doi.org/10.1002/adfm.202007389>

3. T.-Y. Wang, J.-L. Meng, L. Chen, H. Zhu, Q.-Q. Sun et al., Flexible 3D memristor array for binary storage and multi-states neuromorphic computing applications. *InfoMat* **3**(2), 212–221 (2021). <https://doi.org/10.1002/inf2.12158>
4. Z. Zhang, Z. Wang, T. Shi, C. Bi, F. Rao et al., Memory materials and devices: from concept to application. *InfoMat* **2**(2), 261–290 (2020). <https://doi.org/10.1002/inf2.12077>
5. S. Mandal, A. El-Amin, K. Alexander, B. Rajendran, R. Jha, Novel synaptic memory device for neuromorphic computing. *Sci. Rep.* **4**, 5333 (2014). <https://doi.org/10.1038/srep05333>
6. W. Li, T. Mu, Y. Chen, M. Dai, P. Sun et al., Investigation of non-volatile and photoelectric storage characteristics for MoS₂/h-BN/graphene heterojunction floating-gate transistor with the different tunneling layer thicknesses. *Micro. Nano-structures* **187**, 207764 (2024). <https://doi.org/10.1016/j.microna.2024.207764>
7. L. Wu, A. Wang, J. Shi, J. Yan, Z. Zhou et al., Atomically sharp interface enabled ultrahigh-speed non-volatile memory devices. *Nat. Nanotechnol.* **16**(8), 882–887 (2021). <https://doi.org/10.1038/s41565-021-00904-5>
8. X. Huang, C. Liu, Z. Tang, S. Zeng, S. Wang et al., An ultra-fast bipolar flash memory for self-activated in-memory computing. *Nat. Nanotechnol.* **18**(5), 486–492 (2023). <https://doi.org/10.1038/s41565-023-01339-w>
9. X. Hou, C. Liu, Y. Ding, L. Liu, S. Wang et al., A logic-memory transistor with the integration of visible information sensing-memory-processing. *Adv. Sci.* **7**(21), 2002072 (2020). <https://doi.org/10.1002/advs.202002072>
10. W. Li, J. Li, Y. Chen, Z. Chen, W. Li et al., Demonstration of nonvolatile storage and synaptic functions in all-two-dimensional floating-gate transistors based on MoS₂ channels. *ACS Appl. Electron. Mater.* **5**(8), 4354–4362 (2023). <https://doi.org/10.1021/acsaem.3c00595>
11. C. Liu, P. Zhou, Memory devices based on van der Waals heterostructures. *ACS Mater. Lett.* **2**(9), 1101–1105 (2020). <https://doi.org/10.1021/acsmaterialslett.0c00227>
12. K. Chang, B. Hyun, K. Hong, K. Young, J. Won, Memristive devices based on two-dimensional transition metal chalcogenides for neuromorphic computing. *Nano-Micro Lett.* **14**(1), 58 (2022). <https://doi.org/10.1007/s40820-021-00784-3>
13. M.S. Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S.H. Lee et al., Controlled charge trapping by molybdenum disulphide and graphene in ultrathin heterostructured memory devices. *Nat. Commun.* **4**, 1624 (2013). <https://doi.org/10.1038/ncomm s2652>
14. Q.A. Vu, H. Kim, V.L. Nguyen, U.Y. Won, S. Adhikari et al., A high-on/off-ratio floating-gate memristor array on a flexible substrate via CVD-grown large-area 2D layer stacking. *Adv. Mater.* **29**(44), 1703363 (2017). <https://doi.org/10.1002/adma.201703363>
15. J. Kim, Y. Park, J. Lee, E. Lim, J.-K. Lee et al., Impact of HfO₂ dielectric layer placement in Hf_{0.5}Zr_{0.5}O₂-based ferroelectric tunnel junctions for neuromorphic applications. *Adv. Mater. Technol.* **9**(10), 2400050 (2024). <https://doi.org/10.1002/admt.202400050>
16. B. Mukherjee, A. Zulkefli, K. Watanabe, T. Taniguchi, Y. Wakayama et al., Laser-assisted multilevel non-volatile memory device based on 2D van-der-Waals few-layer- ReS_2 /h-BN/graphene heterostructures. *Adv. Funct. Mater.* **30**(42), 2001688 (2020). <https://doi.org/10.1002/adfm.202001688>
17. L. Liu, C. Liu, L. Jiang, J. Li, Y. Ding et al., Ultrafast non-volatile flash memory based on van der Waals heterostructures. *Nat. Nanotechnol.* **16**(8), 874–881 (2021). <https://doi.org/10.1038/s41565-021-00921-4>
18. S. Lakshmy, B. Mondal, N. Kalarikkal, C.S. Rout, B. Chakraborty, Recent developments in synthesis, properties, and applications of 2D Janus MoS₂ and MoSe_xS_(1-x) alloys. *Adv. Powder Mater.* **3**(4), 100204 (2024). <https://doi.org/10.1016/j.apmate.2024.100204>
19. Z. Liu, S.Y. Tee, G. Guan, M.-Y. Han, Atomically substitutional engineering of transition metal dichalcogenide layers for enhancing tailored properties and superior applications. *Nano-Micro Lett.* **16**(1), 95 (2024). <https://doi.org/10.1007/s40820-023-01315-y>
20. D.G. Purdie, N.M. Pugno, T. Taniguchi, K. Watanabe, A.C. Ferrari et al., Cleaning interfaces in layered materials heterostructures. *Nat. Commun.* **9**, 5387 (2018). <https://doi.org/10.1038/s41467-018-07558-3>
21. P.-Y. Chen, X. Peng, S. Yu, NeuroSim: a circuit-level macro model for benchmarking neuro-inspired architectures in online learning. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **37**(12), 3067–3080 (2018). <https://doi.org/10.1109/TCAD.2018.2789723>
22. P.-Y. Chen, X. Peng, S. Yu, NeuroSim+: an integrated device-to-algorithm framework for benchmarking synaptic devices and array architectures, in *2017 IEEE International Electron Devices Meeting (IEDM)*, 6.1.1–6.1.4. IEEE (2018). <https://doi.org/10.1109/iedm.2017.8268337>
23. G. Kresse, J. Furthmüller, Efficiency of ab-initio total energy calculations for metals and semiconductors using a plane-wave basis set. *Comput. Mater. Sci.* **6**(1), 15–50 (1996). [https://doi.org/10.1016/0927-0256\(96\)00008-0](https://doi.org/10.1016/0927-0256(96)00008-0)
24. J.P. Perdew, K. Burke, M. Ernzerhof, Generalized gradient approximation made simple. *Phys. Rev. Lett.* **77**(18), 3865–3868 (1996). <https://doi.org/10.1103/physrevlett.77.3865>
25. P.E. Blöchl, Projector augmented-wave method. *Phys. Rev. B* **50**(24), 17953–17979 (1994). <https://doi.org/10.1103/physrevb.50.17953>
26. S.L. Dudarev, G.A. Botton, S.Y. Savrasov, C.J. Humphreys, A.P. Sutton, Electron-energy-loss spectra and the structural stability of nickel oxide: an LSDA+U study. *Phys. Rev. B* **57**(3), 1505–1509 (1998). <https://doi.org/10.1103/physrevb.57.1505>
27. M. Wu, X. Yao, Y. Hao, H. Dong, Y. Cheng et al., Electronic structures, magnetic properties and band alignments of 3d transition metal atoms doped monolayer MoS₂. *Phys. Lett. A* **382**(2–3), 111–115 (2018). <https://doi.org/10.1016/j.physleta.2017.10.024>

28. S.Y. Park, D.-B. Seo, H. Choi, J.H. Lee, D.H. Lee et al., Structural instability stimulated heteroatoms co-doping of 2D quaternary semiconductor for optoelectronic applications. *Adv. Funct. Mater.* **34**(13), 2310178 (2024). <https://doi.org/10.1002/adfm.202310178>

29. A. Kanwal, A. Jalil, R.A. Raza, S. Ahmed, T. Zhao et al., Effect of strain on electronic properties of tri-layer MoS₂/h-BN/graphene van der Waals heterostructures. *J. Phys. Chem. Solids* **185**, 111776 (2024). <https://doi.org/10.1016/j.jpcs.2023.111776>

30. S.W. Kim, S.Y. Choi, S.H. Lim, E.B. Ko, S. Kim et al., Understanding solvent-induced delamination and intense water adsorption in Janus transition metal dichalcogenides for enhanced device performance. *Adv. Funct. Mater.* **34**(8), 2308709 (2024). <https://doi.org/10.1002/adfm.202308709>

31. D.B. Trivedi, G. Turgut, Y. Qin, M.Y. Sayyad, D. Hajra et al., Room-temperature synthesis of 2D Janus crystals and their heterostructures. *Adv. Mater.* **32**(50), e2006320 (2020). <https://doi.org/10.1002/adma.202006320>

32. M. Lee, T.W. Kim, C.Y. Park, K. Lee, T. Taniguchi et al., Graphene bridge heterostructure devices for negative differential transconductance circuit applications. *Nano-Micro Lett* **15**(1), 22 (2022). <https://doi.org/10.1007/s40820-022-01001-5>

33. C. Acal, D. Maldonado, A.M. Aguilera, K. Zhu, M. Lanza et al., Holistic variability analysis in resistive switching memories using a two-dimensional variability coefficient. *ACS Appl. Mater. Interfaces* **15**(15), 19102–19110 (2023). <https://doi.org/10.1021/acsami.2c22617>

34. K. Jiang, S. Li, F. Chen, L. Zhu, W. Li, Microstructure characterization, phase transition, and device application of phase-change memory materials. *Sci. Technol. Adv. Mater.* **24**, 2252725 (2023). <https://doi.org/10.1080/14686996.2023.2252725>

35. H. Wang, H. Guo, R. Guzman, N. JiaziLa, K. Wu et al., Ultrafast non-volatile floating-gate memory based on all-2D materials. *Adv. Mater.* **36**(24), e2311652 (2024). <https://doi.org/10.1002/adma.202311652>

36. J. Yu, H. Wang, F. Zhuge, Z. Chen, M. Hu et al., Simultaneously ultrafast and robust two-dimensional flash memory devices based on phase-engineered edge contacts. *Nat. Commun.* **14**(1), 5662 (2023). <https://doi.org/10.1038/s41467-023-41363-x>

37. P. Yang, D. Wang, X. Zhao, W. Quan, Q. Jiang et al., Epitaxial growth of inch-scale single-crystal transition metal dichalcogenides through the patching of unidirectionally orientated ribbons. *Nat. Commun.* **13**(1), 3238 (2022). <https://doi.org/10.1038/s41467-022-30900-9>

38. S.-J. Jeong, Y. Gu, J. Heo, J. Yang, C.-S. Lee et al., Thickness scaling of atomic-layer-deposited HfO₂ films and their application to wafer-scale graphene tunnelling transistors. *Sci. Rep.* **6**, 20907 (2016). <https://doi.org/10.1038/srep20907>

39. Z. Zhou, Z. Zhang, P. Li, Z. Guan, Y. Li et al., Low energy consumption photoelectric memristors with multi-level linear conductance modulation in artificial visual systems application. *Nano-Micro Lett.* **17**(1), 317 (2025). <https://doi.org/10.1007/s40820-025-01816-y>

40. J. Sung, S.W. Kim, D. Lee, S. Moon, E. Lee et al., Co-stimuli-driven 2D WSe₂ optoelectronic synapses for neuromorphic computing. *Small* **21**(31), e2504024 (2025). <https://doi.org/10.1002/smll.202504024>

41. J. Hwang, J. Sung, E. Lee, W. Choi, A heterointerface effect of Mo_{1-x}W_xS₂-based artificial synapse for neuromorphic computing. *Chem. Eng. J.* **510**, 161622 (2025). <https://doi.org/10.1016/j.cej.2025.161622>

42. D. Lee, M. Kim, S. Park, S. Lee, J. Sung et al., Inter-ion mutual repulsion control for nonvolatile artificial synapse. *Adv. Funct. Mater.* **35**(11), 2412012 (2025). <https://doi.org/10.1002/adfm.202412012>

43. R.S. Zucker, W.G. Regehr, Short-term synaptic plasticity. *Annu. Rev. Physiol.* **64**, 355–405 (2002). <https://doi.org/10.1146/annurev.physiol.64.092501.114547>

44. J. Sung, H.J. Cheon, D. Lee, S. Chung, L. Ayuningtias et al., Improving ion uptake in artificial synapses through facilitated diffusion mechanisms. *Mater. Horiz.* **12**(14), 5225–5235 (2025). <https://doi.org/10.1039/d5mh00005j>

45. J. Sung, S. Chung, Y. Jang, H. Jang, J. Kim et al., Unveiling the role of side chain for improving nonvolatile characteristics of conjugated polymers-based artificial synapse. *Adv. Sci.* **11**(16), 2400304 (2024). <https://doi.org/10.1002/advs.20240304>

46. H. Zhou, S. Li, K.-W. Ang, Y.-W. Zhang, Recent advances in in-memory computing: exploring memristor and memtransistor arrays with 2D materials. *Nano-Micro Lett.* **16**(1), 121 (2024). <https://doi.org/10.1007/s40820-024-01335-2>

47. K. Wang, S. Ren, Y. Jia, X. Yan, L. Wang et al., MXene-Ti₃C₂T_x-based neuromorphic computing: physical mechanisms, performance enhancement, and cutting-edge computing. *Nano-Micro Lett.* **17**(1), 273 (2025). <https://doi.org/10.1007/s40820-025-01787-0>

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.