CrossMark

ARTICLE

Observation of Resistive Switching Memory by Reducing Device Size in a New Cr/CrO$_x$/TiO$_x$/TiN Structure

Debanjan Jana[1] · Subhranu Samanta[1] · Sourav Roy[1] · Yu Feng Lin[1] · Siddheswar Maikap[1]

Abstract The resistive switching memory characteristics of 100 randomly measured devices were observed by reducing device size in a Cr/CrO$_x$/TiO$_x$/TiN structure for the first time. Transmission electron microscope image confirmed a via-hole size of 0.4 μm. A 3-nm-thick amorphous TiO$_x$ with 4-nm-thick polycrystalline CrO$_x$ layer was observed. A small 0.4-μm device shows reversible resistive switching at a current compliance of 300 μA as compared to other larger size devices (1–8 μm) owing to reduction of leakage current through the TiO$_x$ layer. Good device-to-device uniformity with a yield of >85 % has been clarified by weibull distribution owing to higher slope/shape factor. The switching mechanism is based on oxygen vacancy migration from the CrO$_x$ layer and filament formation/rupture in the TiO$_x$ layer. Long read pulse endurance of >10^5 cycles, good data retention of 6 h, and a program/erase speed of 1 μs pulse width have been obtained.

Keywords CrO$_x$ · TiO$_x$ · Resistive switching memory · Slope/shape factor · Device size

1 Introduction

Recently resistive random access memory (RRAM) has been investigated for the next-generation non-volatile memory applications [1, 2]. The RRAM device offers a promise for NVM application due to its simple structure, low power consumption, high density, fast program/erase speed, and low cost [3]. Various materials like HfO$_x$ [4], TaO$_x$ [5, 6], TiO$_x$ [7–10], and so on have been reported by many groups. Other materials such as ZnO [11], BaWO$_4$ [12], and so on have been reported also. Among of them, TiO$_x$ is one of the most promising materials owing to its fab-friendly, good thermal stability, adequate band gap (∼3.0 eV) for low leakage, high dielectric constant (κ ∼ 80), and so on [13]. Kwon et al. [14] have reported the bipolar resistive switching in Pt/TiO$_2$/Pt structure at a

high current compliance (CC) of 30 mA. Jeong et al. [15] have reported the bilayer switching layers in a Pt/Ni/a-TiO$_2$/Al$_2$O$_3$/Pt structure with a CC of >1 mA. Park et al. [16] have unveiled the multi-bit resistive switching operation in an Ir/TiO$_x$/TiN structure with a CC of 1 mA. Goren et al. [17] demonstrated bistable memory effect in Co/TiO$_2$/TiO$_x$/Co/Pd structure with a low CC of approximately 100 μA. Zeng et al. [18] have reported resistive switching characteristics using a Pt/ZrO$_2$/TiO$_2$/Pt structure at a CC of 10 mA. Strachan et al. [19] have reported the resistive switching characteristics using a Cr/Pt/TiO$_2$/Pt structure at a CC of 250 μA.

Although many groups have reported these TiO$_x$-based different RRAM devices, however, resistive switching characteristics by reducing device size as well as leakage current in a Cr/CrO$_x$/TiO$_x$/TiN structure have not been investigated yet. To obtain good resistive switching characteristics, both amorphous TiO$_x$ switching and polycrystalline CrO$_x$ oxygen vacancy supply layers are effectively combined with smaller device sizes. Microstructure and device size are confirmed by transmission electron microscope (TEM) image. The switching mechanism is owing to oxygen vacancy filament formation/rupture into the TiO$_x$

✉ Siddheswar Maikap
sidhu@mail.cgu.edu.tw

[1] Thin Film Nano Tech. Lab., Department of Electronic Engineering, Chang Gung University, 259 Wen-Hwa 1st Rd., Kwei-Shan, Tao-Yuan 333, Taiwan, ROC

switching layer. Weibull distribution plot of 100 randomly measured devices with a size of 0.4×0.4 μm^2 shows good device-to-device uniformity with a yield of >85 %. It is found that higher slope/shape factor indicates higher uniformity of the devices. By investigating the scale factor, it is found that the device can be operated with low voltage of ± 1 V and a low current of <300 μA. Long read pulse endurance of >10^5 cycles, stable data retention of >6 h, and good program/erase (P/E) endurance with a pulse width of 1 μs are obtained, which indicate future application of this new $Cr/CrO_x/TiO_x/TiN$ resistive switching memory device.

2 Experimental

The $Cr/CrO_x/TiO_x/TiN$ RRAM devices were fabricated using 8-inch SiO_2/Si wafers. The device process flow is shown in Fig. 1. The thickness of SiO_2 layer was 200 nm. A 200-nm-thick titanium-nitride (TiN) as a bottom electrode (BE) was deposited on SiO_2 layer. Next 150-nm-thick SiO_2 layer was deposited to different pattern via-hole sizes ranging from 0.4×0.4 to 8×8 μm^2 using both photolithography and dry etching processes. Then, 8 inch wafer was broken to 2×2 $inch^2$ pieces and did next step.

The chromium (Cr) metal as a top electrode (TE) was deposited by radio frequency (RF) sputtering. The Cr metal target with a constant argon (Ar) gas flow rate of ten sccm was used. During deposition, chamber pressure and deposition power were 6 mTorr and 100 W, respectively. A TiO_x resistive switching layer with a CrO_x layer was observed after deposition of Cr TE. Finally, lift-off process was done to get a simple $Cr/CrO_x/TiO_x/TiN$ structure. More than 150 devices for each size were obtained on a small piece of 8 inch wafer.

The memory characteristics were investigated by measuring 100 randomly picked devices. Thickness and microscopic structure of $Cr/CrO_x/TiO_x/TiN$ RRAM device were analyzed by transmission electron microscopy with energy of 200 keV. Electrical characteristics were measured by Agilent 4156C/B1500 precision semiconductor analyzer. During measurement, the bias was applied on the TE and the BE was grounded.

3 Results and Discussion

Figure 2a shows TEM image of a typical via-hole size of 0.4×0.4 μm^2. The length of via-hole is found to be approximately 0.5 μm. A thickness of Cr layer is
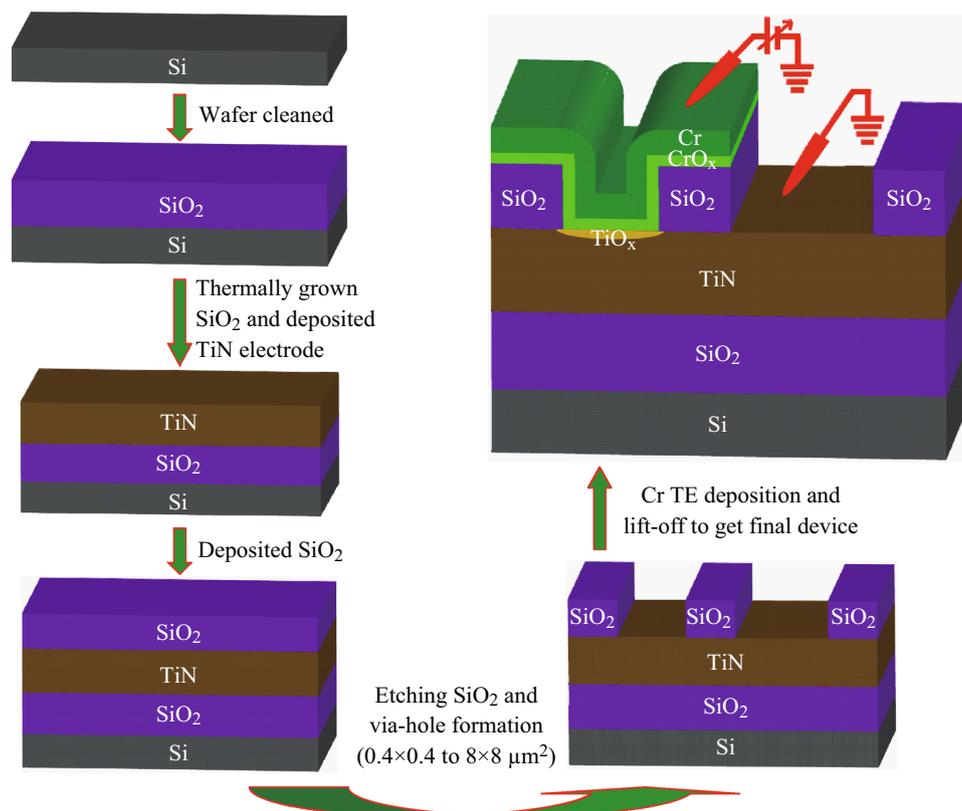
Fig. 1 The RRAM device with sizes ranging from 0.4×0.4 to 8×8 μm^2

394

Nano-Micro Lett. (2015) 7(4):392–399
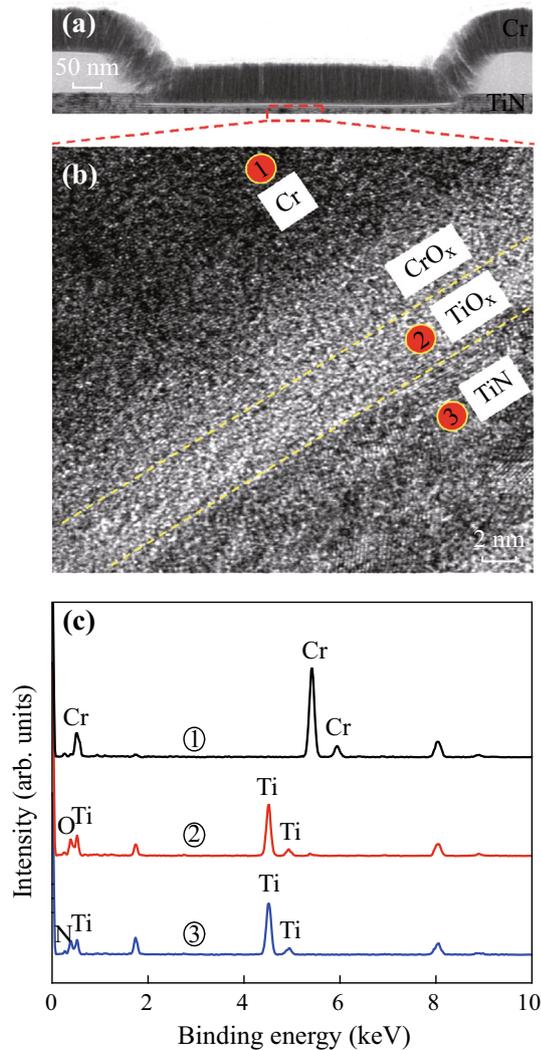
Fig. 2 a TEM image of Cr/CrO$_x$/TiO$_x$/TiN RRAM device with a via-hole size of 0.4-μm device. **b** HRTEM image shows a CrO$_x$ layer in between TiO$_x$ switching and Cr electrode because of partially oxidization of Cr metal during deposition. **c** EDX spectrum confirms the presence of Cr, Ti, O, and N elements in *1*, *2*, and *3* denoted layers of (**b**)

approximately 150 nm. High-resolution TEM image on inside via-hole region confirms the layer-by-layer of Cr/CrO$_x$/TiO$_x$/TiN structure (Fig. 2b). The thickness of amorphous TiO$_x$ layer is approximately 3 nm, which acts as a switching layer. This TiO$_x$ layer is grown during the Cr TE deposition owing to lower Gibbs free energy of TiO$_2$ (-887.6 kJ (mol)$^{-1}$ at 300 K). In addition, reactive Cr TE is also partially oxidized at the Cr/TiO$_x$ interface and creates CrO$_x$ owing to lower Gibbs free energy of Cr$_2$O$_3$ of -694.88 kJ (mol)$^{-1}$ [20, 21]. This CrO$_x$ layer with a thickness of approximately 4 nm is polycrystalline. Elemental analysis of Cr/CrO$_x$/TiO$_x$/TiN structure has been explored by EDX spectrum. The existence of Cr, Ti, O, N elements in corresponding layers of 1, 2, 3 are shown in

Fig. 2c. The peaks' position of Cr, Ti, O, N elements are found to be 5.4, 4.5, 0.4, and 0.28 keV, respectively. Due to both lower Gibbs free energy and deposition by sputtering, the defective CrO$_x$ layer is formed or oxygen vacancy is observed in the CrO$_x$ layer. Therefore, this CrO$_x$ layer acted as an oxygen vacancy supply layer to form conductive filament into the TiO$_x$ switching layer and good switching characteristics can be observed below.

Figure 3a exhibits the current–voltage (I–V) switching characteristics of a 0.4-μm device at a CC of 300 μA. Voltage sweeping direction is shown by arrows 1–4. The device requires a very small forming voltage (V_{form}) of 0.9 V because of both thin TiO$_x$ switching layer and vacancy supply from the CrO$_x$ layer. Small SET (V_{SET}) and RESET voltages (V_{RESET}) are found to be 0.6 and -0.6 V, respectively. The RESET currents are found to be 314 and 391 μA for first and second cycle, respectively.

Cumulative probability of RESET currents for the first and second cycles is shown in Fig. 3b. At a 50 % probability, the RESET currents are found to be 329 and 344 μA for 1st and 2nd cycles, respectively. The RESET current is slightly higher (~ 15 %) than current compliance owing to small current overshoot effect, which can be reduced by optimizing operation current. Further study is needed to evaluate this effect. This current overshoot effect is happening during formation or SET of the devices. Therefore, this structure provides good current clamping and minimizes current overshoot effects, even a one-resistor (1R) configuration.

Cumulative probability of initial resistance state (IRS), high resistance state (HRS), and low resistance state (LRS) for three different device sizes of 0.4, 1, and 8 μm is shown in Fig. 3c. The average values of IRS are 457.5, 46.5, and 670 Ω for the 0.4-, 1-, and 8-μm devices, respectively. The leakage currents increase with increasing device sizes, which are owing to the presence of much higher amount of defects or oxygen vacancies (V_o) in larger device sizes. The average values of HRS/LRS are 144/2.7, 1.5/1.2 kΩ, and 188/175 Ω for 0.4, 1, and 8 μm, respectively at a read voltage (V_{read}) of 0.2 V. This implies that large size devices (1 and 8 μm) do not show the bipolar resistive switching at a low CC of 300 μA. By reducing the device size as well as leakage current, good resistive switching characteristics could be observed even a simple structure has been designed and fabricated here. In addition, it is found that a non-zero current of approximately 2×10^{-7} A is observed at initial and high resistance state, which might possibly be due to capacitive effect. However, a further study is needed.

Figure 4a shows weibull distribution of IRS, HRS, and LRS for the 0.4-μm devices. These narrow dispersion values interpret that device-to-device uniformity is good with a yield (i.e., switchable devices with consecutive 2
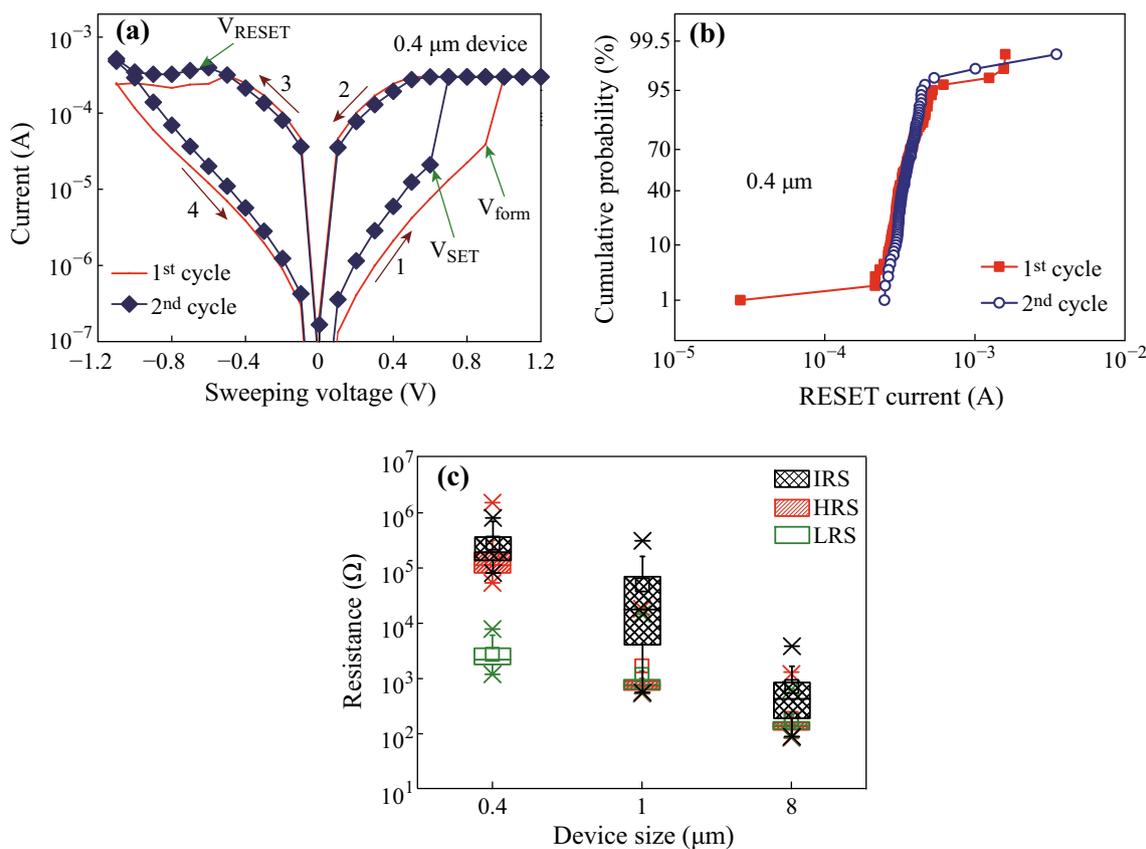
Fig. 3 Current–voltage characteristics with device size-dependence switching of 100 measured devices. **a** Bipolar *I–V* switching characteristics. **b** Cumulative probability of RESET currents for 0.4-μm device at a low CC of 300 μA, **c** Box chart plot of IRS, HRS, and LRS of 0.4, 1, and 8 μm devices. *Error bars* mean a range of total data distribution

cycles and resistance ratio is >2) of 85 %. We can justify successive switching devices or reliability test as follows by weibull distribution plot [22]. Mathematically, this can be expressed as

$$W(Q) = \ln[-\ln(1 - F)], \tag{1}$$

$$F(Q) = 1 - \exp\left[-\left(\frac{Q}{\alpha_{63\%}}\right)^{\beta}\right], \tag{2}$$

where $F(Q)$ is the cumulative distribution function of failure, Q is the values of measured data, β is the slope value of weibull distribution curve or shape factor which signifies the statistical dispersion of data, and $\alpha_{63\%}$ is the scale factor value from weibull distribution at approximately $F = 63$ %. Higher β value means that distribution is more uniform. The uniform distribution means that the fitting line should be perpendicular on *X*-axis. Using Eq. (1), weibull distribution patterns of IRS, HRS, LRS, V_{form}, V_{SET}, and V_{RESET} for the 0.4-μm devices have been depicted in Fig. 4. Using Eq. (2), the values of β are found to be from the fitting curves, as shown by straight line. The β value of LRS (2.5) distribution is narrower than those of

both HRS (1.84) and IRS (1.1), as listed values in Table 1. In addition, IRS distribution of the 0.4-μm devices is narrowest as compared to widely scattered β values for 1-μm (0.46) and 8-μm (0.96) devices (not shown here), which may also related to the higher leakage.

It is found that the average values of V_{form}, V_{SET}, V_{RESET} for the 0.4-μm devices are 0.9, 0.7, and −0.54 V, respectively. As compared to the V_{SET}, a small V_{form} of 0.9 V is necessary to switch a pristine device or it is like a forming-free device, which is very useful for integrated circuit (IC) application and saving extra device process step as well as low cost. The formation step can be avoided by reducing voltage of <3 V then the device will be used directly after fabrication. A 3 V battery can be used directly to program/ erase this memory device or extra voltage amplifier which is used in Flash memory is not needed. The β values of V_{form}, V_{SET}, and V_{RESET} are 10.4, 7.34, and 3.9 (Fig. 4b–d), which suggests that formation of the devices is more uniform than those of the SET and RESET voltages. The values of standard deviation of V_{form}, V_{SET}, and V_{RESET} are 0.174, 0.189, and 0.139, respectively, which assert good device-to-device uniformity yield.
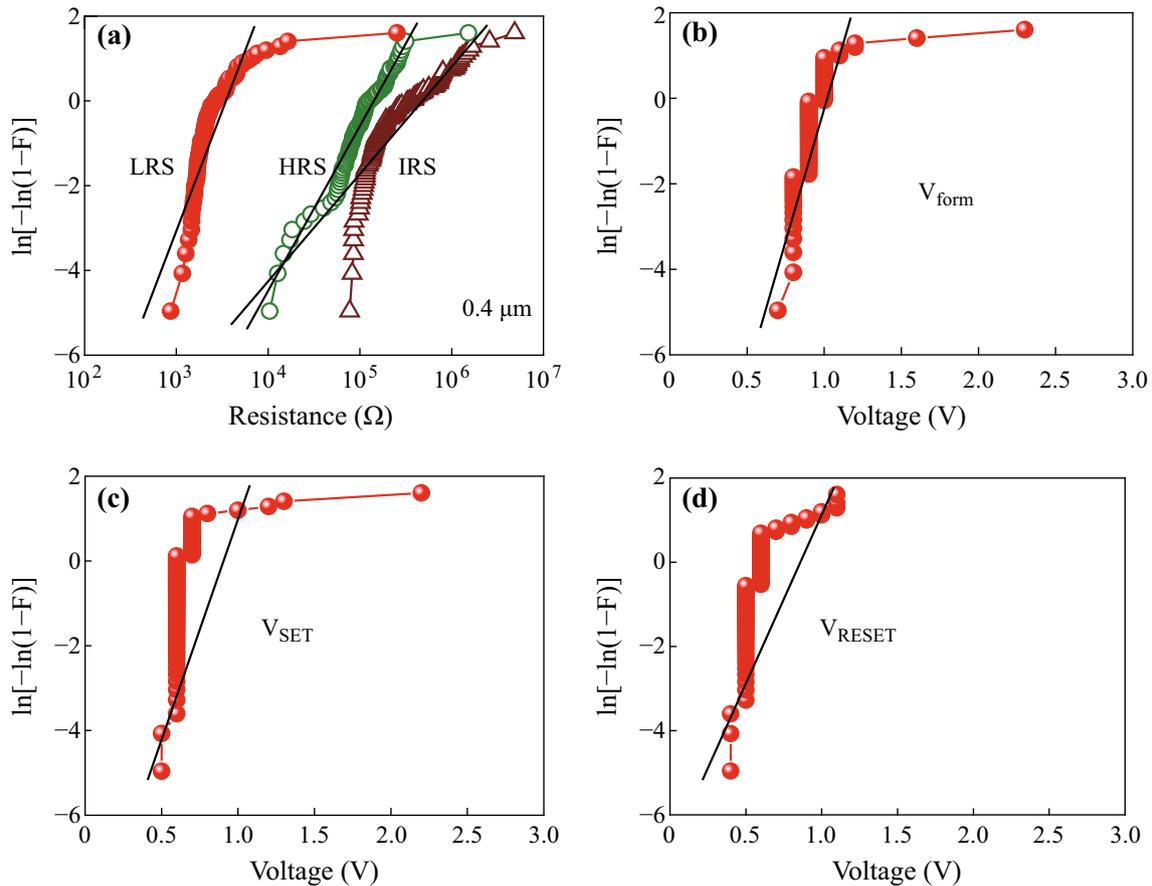
Fig. 4 Weibull distribution of **a** IRS, HRS, and LRS, **b** formation, **c** SET, and **d** RESET voltages for 100 arbitrary picked 0.4-μm devices

Table 1 Values of β and $\alpha_{63\%}$ for the Cr/CrO$_x$/TiO$_x$/TiN with a device size of 0.4 μm

Parameters	Slope/shape factor (β)	Scale factor ($\alpha_{63\%}$)
IRS	1.1	431.5 kΩ
HRS	1.84	139.5 kΩ
LRS	2.5	6 kΩ
V_{form}	10.4	0.97 V
V_{SET}	7.34	0.66 V
V_{REST}	3.9	−0.64 V

The values of scale factor ($\alpha_{63\%}$) for the HRS and LRS are found to be 139.5 and 6 kΩ, respectively. A resistance ratio of approximately 20 is obtained. For a single bit operation, a resistance ratio of >2 is enough to indentify '0' and '1' states [1, 3, 23]. The higher resistance ratio is better for MLC operation. Therefore, scientists are as large as resistance ratio with maintaining other memory parameters, which is also good for future application. The values of $\alpha_{63\%}$ for the V_{form}, V_{SET}, and V_{RESET} are found to be 0.97, 0.66, and −0.64 V, respectively. This suggests that the device could be operated at low voltage of ±1 V.

To evaluate the current conduction mechanism, LRS shows ohmic and HRS shows the space-charge-limited current conduction (SCLC). Stochastic filament formation in TiO$_x$ layer by oxygen vacancy will lead to respond to the ohmic nature of LRS. On the other hand, injected electrons through the electrodes are exceeded than those thermally generated free electrons in the TiO$_x$ layer. Therefore, oxygen vacancy filament formation/rupture into the TiO$_x$ layer under external bias is the switching mechanism, which is also reported by other research groups in different structures [14, 19, 24]. In the Cr/CrO$_x$/TiO$_x$/TiN structure, when positive bias is applied on the Cr TE then the potential is distributed in series of TiO$_x$ and CrO$_x$ layers. It is true that TiO$_x$ layer has more insulating property than the CrO$_x$ layer. Therefore, the potential drop on a pristine device is higher across the TiO$_x$ layer. Then, Ti–O bonds start to break and electrical conductivity of the TiO$_x$ layer is increased. In this situation, the potential drop ($V > V_{form} > V_{SET}$) across CrO$_x$ layer is increased, which results in the oxygen vacancies as a positive charge in the CrO$_x$ layer moving towards TiO$_x$ layer as well as the V_o filament is formed into the TiO$_x$ layer (Fig. 5a). The device
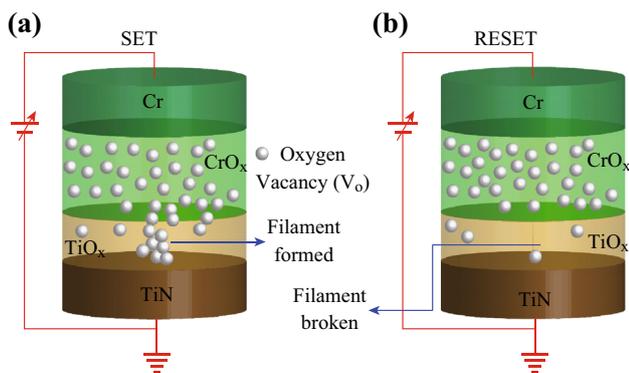
Fig. 5 Schematic illustration of switching mechanism. **a** Under SET operation, the oxygen vacancy is migrated from CrO_x layer to the TiO_x switching layer and oxygen vacancy conducting filament is formed. **b** Under RESET operation, the oxygen vacancy is moved toward CrO_x layer from the TiO_x layer and the filament is ruptured

switches from IRS (or HRS) to LRS. By applying negative bias ($V < V_{RESET}$) on the Cr TE, the oxygen vacancies attracted toward the TE and stored into the CrO_x layer,

which results that the filament is broken (Fig. 5b). Then, the device switches back from LRS to previous HRS. However, there is difference in between IRS and HRS because of Ti–O bonds break during the formation of filament initially. Due to these CrO_x/TiO_x bilayers' action, repeatable bipolar resistive switching cycles are observed.

To explore the performance potentiality of the $Cr/CrO_x/TiO_x/TiN$ RRAM devices, program/erase (P/E) endurance and data retention characteristics have been evaluated (Fig. 6). The memory device shows long read pulse endurance measured at V_{read} of 0.2 V (Fig. 6a). The device is programed with difference CCs of 300 and 500 μA. After programing the data are read with a pulse width of 500 μs. The LRS values for CCs of 300 and 500 μA are 5 and 3 kΩ, respectively. The value of LRS decreases with increasing current compliance, which can be used as a multi-level cell. After erasing the data are read with a pulse width of 500 μs. The long read pulse endurance of $>10^5$ cycles is obtained. Good data retention of 6 h with a good memory window (HRS/LRS) of approximately 40 can be
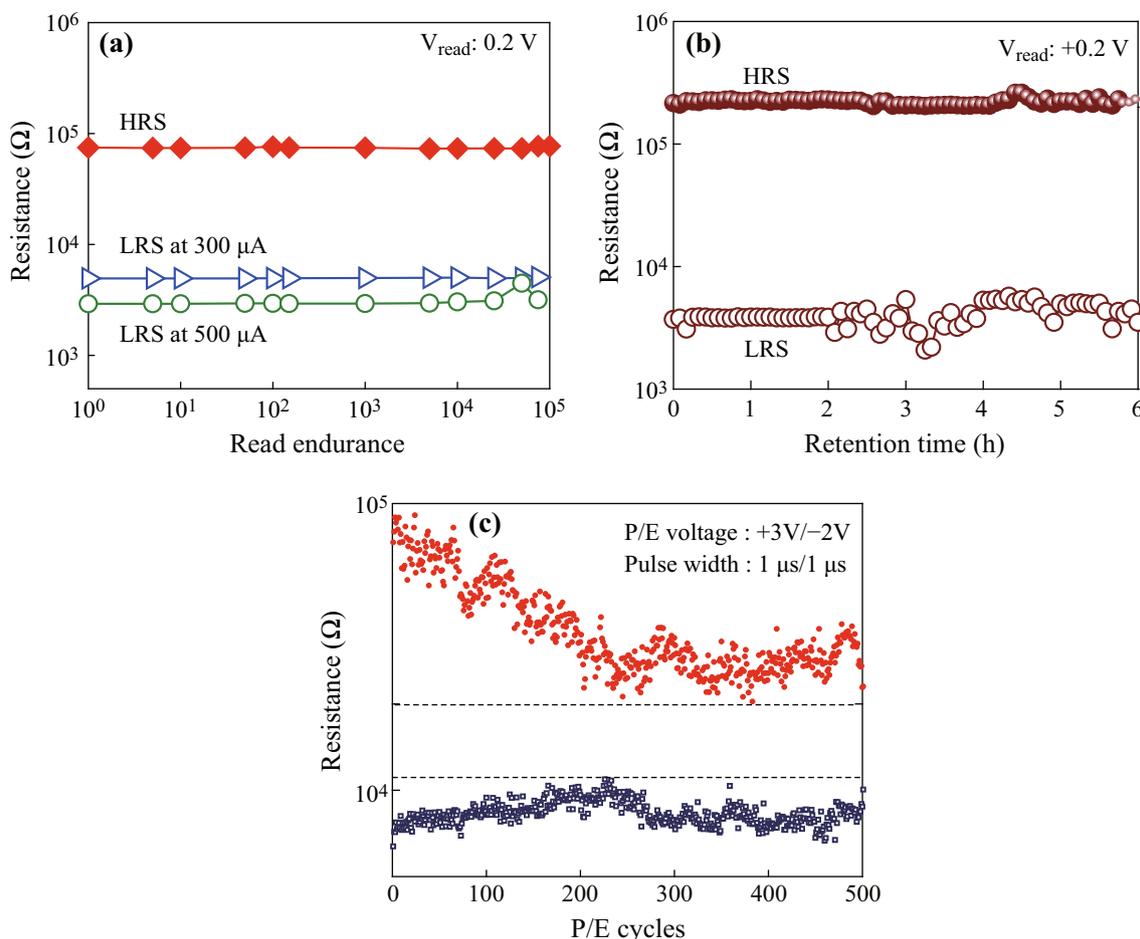
Fig. 6 **a** Long read pulse endurance of $>10^5$ cycles, **b** Stable data retention of 6 h at a CC of 300 μA, and **c** Good endurance of >500 cycles at a small program/erase pulse width of 1/1 μs obtained for this new $Cr/CrO_x/TiO_x/TiN$ RRAM device

398

Nano-Micro Lett. (2015) 7(4):392–399

achieved from this RRAM device (Fig. 6b). This memory device shows good P/E endurance of >500 cycles at V_{read} of 0.2 V (Fig. 6c). A P/E pulse width of 1/1 μs and voltage of 3/−2 V are applied. A small fluctuation of LRS in both data retention and P/E endurance was observed, which can be assumed to be the generation and redistribution of oxygen vacancies in the TiO_x switching layer owing to rapid increasing pulse operation. Shen et al. [25] have also discussed about the P/E endurance failure in Pt/BST/SRO RRAM structure due to generation and redistribution of defects in switching material. Further improvement is needed for P/E cycles. Eventually, this memory device with reducing size has very keen potential for future nanoscale non-volatile memory application.

4 Conclusions

In summary, observation of resistive switching memory by reducing device size as well as leakage current has been revealed in a new $Cr/CrO_x/TiO_x/TiN$ RRAM device. By measuring 100 random devices it is found that a smaller size device has lower leakage current and resistive switching characteristics are observed. Both TEM image and EDX spectrum confirm a device size of 0.4×0.4 μm^2 with the presence of amorphous TiO_x and polycrystalline CrO_x layer is also observed. The 0.4-μm devices can perform resistive switching at a low CC of 300 μA owing to lower leakage current as compared to larger size devices. Weibull plots of IRS, HRS, LRS, V_{form}, V_{SET}, and V_{RESET} show that more than 85 % devices have good switching with tight distribution. The slope/shape factor indicates the device uniformity. The resistive switching is due to the formation/rupture of oxygen vacancy filament in the TiO_x switching layer and the CrO_x layer acts as a vacancy supply layer. Therefore, long read pulse endurance of >10^5 cycles, data retention of >6 h, and P/E endurance of >500 cycles with a pulse width of 1 μs at a low operation current of 300 μA are obtained. It is concluded that a new $Cr/CrO_x/TiO_x/TiN$ RRAM device has a simple fabrication process and good resistive switching memory characteristics, which will be very promising for future nanoscale non-volatile memory application.

References

1. F. Pan, S. Gao, C. Chen, S. Song, F. Zeng, Recent progress in resistive random access memories: materials, switching mechanisms, and performance. Mater. Sci. Eng. R **83**, 1–59 (2014). doi:10.1016/j.mser.2014.06.002

2. K. Terabe, T. Hasegawa, T. Nakayama, M. Aono, Quantized conductance atomic switch. Nature **433**, 47–50 (2005). doi:10.1038/nature03190

3. R. Waser, M. Aono, Nanoionics-based resistive switching memories. Nat. Mater. **6**, 833–840 (2007). doi:10.1038/nmat2023

4. B. Govoreanu, G.S. Kar, Y-Y. Chen, V. Paraschiv, S. Kubicek, et al., 10×10 nm^2 Hf/HfO$_x$ crossbar resistive RAM with excellent performance, reliability and low-energy operation. Electron Devices Meeting (IEDM), 31.6.1–31.6.4. (2011). doi:10.1109/IEDM.2011.6131652

5. M.-J. Lee, C.B. Lee, D. Lee, S.R. Lee, M. Chang et al., A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta$_2$O$_{5−x}$/TaO$_{2−x}$ bilayer structures. Nat. Mater. **10**, 625–630 (2011). doi:10.1038/nmat3070

6. A. Prakash, D. Jana, S. Maikap, TaOx–based resistive switching memories: prospective and challenges. Nanoscale Res. Lett. **8**, 418 (2013). doi:10.1186/1556-276X-8-418

7. B.J. Choi, D.S. Jeong, S.K. Kim, C. Rohde, S. Choi et al., Resistive switching mechanism of TiO$_2$ thin films grown by atomic-layer deposition. J. Appl. Phys. **98**, 033715 (2005). doi:10.1063/1.2001146

8. J.J. Yang, M.D. Pickett, X. Li, D.A.A. Ohlberg, D.R. Stewart, R.S. Williams, Memristive switching mechanism for metal/oxide/metal nanodevices. Nat. Nanotechnol. **3**, 429–433 (2008). doi:10.1038/nnano.2008.160

9. C. Hermes, R. Bruchhaus, R. Waser, Forming-free TiO$_2$-based resistive switching devices on CMOS-compatible W-plugs. IEEE Electron Device Lett. **32**(11), 1588–1590 (2011). doi:10.1109/LED.2011.2166371

10. L. Qingjiang, A. Khiat, L. Salaoru, C. Papavassiliou, X. Hui, T. Prodomakis, Memory impedance in TiO$_2$ based metal-insulator-metal devices. Sci. Rep.-UK **4**, 4522 (2014). doi:10.1038/srep04522

11. L. Li, Y. Zhang, Z. Chew, A Cu/ZnO nanowire/Cu resistive switching device. Nano-Micro Lett. **5**(3), 159–162 (2013). doi:10.1007/BF03353745

12. B. Sun, Y. Liu, W. Zhao, J. Wu, P. Chen, Hydrothermal preparation and white-light controlled resistive switching behavior of BaWO$_4$ nanospheres. Nano-Micro Lett. **7**(1), 80–85 (2014). doi:10.1007/s40820-014-0021-5

13. B. Prasai, B. Sai, M.K. Underwood, J.P. Lewis, D.A. Drabold, Properties of amorphous and crystalline titanium dioxide from first principles. J. Mater. Sci. **47**(21), 7515–7521 (2012). doi:10.1007/s10853-012-6439-6

14. D.-H. Kwon, K.M. Kim, J.H. Jang, J.M. Jeon, M.H. Lee et al., Atomic structure of conducting nanofilaments in TiO$_2$ resistive switching memory. Nat. Nanotechnol. **5**, 148–153 (2010). doi:10.1038/nnano.2009.456

15. H.Y. Jeong, J.Y. Lee, S.Y. Choi, Interface-engineered amorphous TiO$_2$-based resistive memory devices. Adv. Funct. Mater. **20**, 3912–3917 (2010). doi:10.1002/adfm.201001254

16. J. Park, M. Jo, S. Jung, J. Lee, W. Lee, S. Kim, S. Park, J. Shin, H. Hwang, New set/reset scheme for excellent uniformity in bipolar resistive memory. IEEE Electron Device Lett. **32**(3), 228–230 (2011). doi:10.1109/LED.2010.2094599

17. E. Goren, M. Ungureanu, R. Zazpe, M. Rozenberg, L.E. Hueso, P. Stoliar, Y. Tsur, F. Casanova, Resistive switching phenomena in TiO$_x$ nanoparticle layers for memory applications. Appl. Phys. Lett. **105**, 143506 (2014). doi:10.1063/1.4897142

18. B. Zeng, D. Xu, M. Tang, Y. Xiao, Y. Zhou, R. Xiong, Z. Li, Y. Zhou, Improvement of resistive switching performance via an amorphous ZrO_2 layer formation in TiO_2-based forming-free resistive random access memory. J. Appl. Phys. **116**, 124514 (2014). doi:10.1063/1.4896402

19. J.P. Strachan, M.D. Pickett, J.J. Yang, S. Aloni, A.L.D. Kilcoyne, G.M. Ribeiro, R.S. Williams, Direct identification of the conducting channels in a functioning memristive device. Adv. Mater. **22**, 3573–3577 (2010). doi:10.1002/adma.201000186

20. W.Y. Chang, H.W. Huang, W.T. Wang, C.H. Hou, Y.L. Chueh, J.R. He, High uniformity of resistive switching characteristics in a Cr/ZnO/Pt device. J. Electrochem. Soc. **159**, G29–G32 (2012). doi:10.1149/2.092203jes

21. N.R. Mann, R.E. Schafer, N.D. Singpurwalla, *Methods for Statistical Analysis of Reliability and Life Data* (Wiley publishers, New York, 1974)

22. K. Kamiya, M.Y. Yang, S.G. Park, B.M. Kope, Y. Nishi, M. Niwa, K. Shiraishi, ON–OFF switching mechanism of resistive-random-access-memories based on the formation and disruption of oxygen conducting channels. Appl. Phys. Lett. **100**, 073502 (2012). doi:10.1063/1.3685222

23. S. Roy, S. Maikap, G. Sreekanth, M. Dutta, D. Jana, Y.Y. Chen, J.R. Yang, Improved resistive switching phenomena and mechanism using Cu–Al alloy in a new Cu:AlO_x/TaO_x/TiN structure. J. Alloy. Compd. **637**, 517–523 (2015). doi:10.1016/j.jallcom.2015.02.168

24. H.H. Pham, L.W. Wang, Oxygen vacancy and hole conduction in amorphous TiO_2. Phys. Chem. Chem. Phys. **17**, 541 (2015). doi:10.1039/C4CP04209C

25. W. Shen, R. Dittmann, U. Breuer, R. Waser, Improved endurance behavior of resistive switching in (Ba, Sr)TiO_3 thin films with W top electrode. Appl. Phys. Lett. **93**, 222102 (2008). doi:10.1063/1.3039809