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Unique Characteristics of Vertical Carbon Nanotube Field-effect Transistors on Silicon

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Abstract: A vertical carbon nanotube field-effect transistor (CNTFET) based on silicon (Si) substrate has been proposed and simulated using a semi-classical theory. A single-walled carbon nanotube (SWNT) and an n-type Si nanowire in series construct the channel of the transistor. The CNTFET presents ambipolar characteristics at positive drain voltage (V_d) and n-type characteristics at negative V_d. The current is significantly influenced by the doping level of n-Si and the SWNT band gap. The n-branch current of the ambipolar characteristics increases with increasing doping level of the n-Si while the p-branch current decreases. The SWNT band gap has the same influence on the p-branch current at a positive V_d and n-type characteristics at negative V_d. The lower the SWNT band gap, the higher the current. However, it has no impact on the n-branch current in the ambipolar characteristics. Thick oxide is found to significantly degrade the current and the subthreshold slope of the CNTFETs.

Keywords: Carbon Nanotube; Field-effect Transistors; Semi-classical Simulation

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Introduction

The rapid development of information technology requires a smaller MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), the main building block in microelectronics. The shrinkage of the MOSFET must follow the Dennard's scaling theory [1], i. e., the vertical dimensions must be scaled down with the lateral dimensions to avoid the so-called short channel effect. This means the channel thickness must be scaled down together with the channel length. However, this shrinkage will stop when it meets the physics limit. It has been reported that the bulk silicon MOSFET will not perform reliably at sub-10 nm gate length [2]. New material or new transistor structure must be developed at the end of scaling road map. Single-walled carbon nanotubes (SWNTs) have been considered to be one of the most promising materials for silicon due to their excellent electrical properties and ultrathin body [3, 4]. The sub-2 nm diameter of the SWCNT makes it easier to satisfy the body thickness requirement for a 5 nm node FET while it is impossible for Si technology [2, 5]. Recently-developed CNTFETs with single SWCNT and sub-10 nm channel length have shown much better performance than the best competing silicon devices [6] in switching behavior and the normalized current density at a low operating voltage of 0.5 V. More importantly, the output characteristics have shown clear device saturation behavior at a drain voltage less than 0.4 V, much lower than the 0.64 V predicted by the ITRS Roadmap for 5 nm node transistors [7], showing the power benefit of CNTFETs compared to silicon transistors.

Despite the promising progress in the performance of the CNTFETs, the fabrication of short channel CNT-

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FETs still rely on some high cost and low throughput techniques, for example, electron beam lithography. To solve this problem, we have developed vertical carbon nanotube field-effect transistors (CNTFETs) recently [8, 9]. The unique feature of this kind of CNTFETs is that the source and drain of the transistors are vertically stacked with a dielectric sandwiched in between. This configuration makes it easier to fabricate short channel CNTFETs because the channel length is precisely the thickness of the dielectric layer between the source and drain. Short channel length in the range from several nanometers to sub-micrometers can be fabricated without using those complicated techniques. Another advantage of this structure is that it can improve the integration density since the vertical transistors occupy less space than their planar counterpart [10]. Furthermore, it offers an approach to integrate carbon nanotubes to silicon if the vertical CNTFETs are fabricated on silicon. This fabrication does not need to change the silicon technology. By using SiN_x to isolate the Si source and metal drain contact, we have successfully fabricated vertical CNTFETs on Si [9], as schematically shown in Fig. 1(a). The channel length and channel width are 600 nm and 2 μm, respectively. The mobility of our CNTFETs is better than other group's results which are extracted from planar CNTFETs fabricated using similar CNT solution [11, 12]. Interestingly, the vertical CNTFETs have shown some characteristics significantly different from those CNTFETs fabricated with metal source and drain. The transfer characteristics of the vertical CNTFETs on Si can be either ambipolar or unipolar (n-type or p-type) depending on the sign of the drain voltages [9]. The n-type/p-type characteristics are defined by the Si doping type. We have simulated these phenomena using a semi-classical model in our former paper [9]. The calculation results are well consistent with the experimental observations. However, the variations of Si doping level and carbon nanotube band gap have not been taken into consideration. In this paper, we will present the influence of different alignment of Si Fermi level and different carbon nanotube band gap, and the impact of the oxide thickness on the performance of the CNTFETs in detail. It is very useful for designing a perfect vertical CNTFET on Si.

1 Methods

The performances of the vertical CNTFETs on Si are simulated using a semi-classical method [13-17]. The configuration of the CNTFET is schematically illustrated in Fig. 1(b). Source and drain are vertically stacked, isolated by SiN_x. Since the gate overlapped with part of the silicon contact in experiment, as shown in Fig. 1(a), the conductance of this part is also modified by the gate voltage. We therefore propose that the channel is composed of a SWNT and a Si nanowire in the calculation. Two metal contacts are used as source and drain of the CNTFET. A grounded right gate electrode (not shown here) is used for the calculations. It is 190 nm away from the HfO_2 gate dielectric layer.

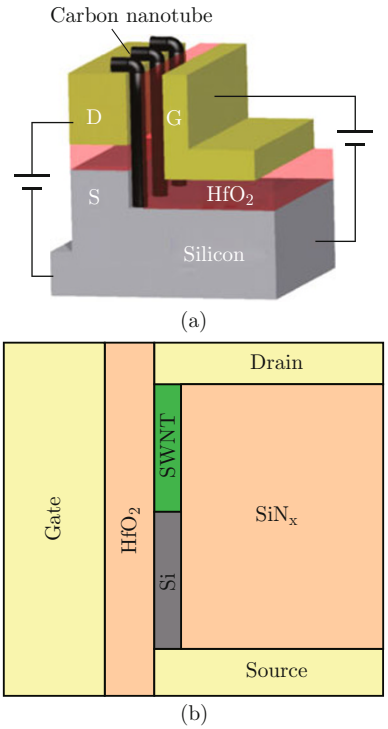

Fig. 1 a) 3D structure of the vertical CNTFET on silicon. b) Schematic configuration of the CNTFET for calculation. The vertical channel is composed of a SWNT and a Si nanowire.

As we know, CNTFETs work as Schottky barrier (SB) transistors [18]. The current is controlled by thermal assisted tunneling through the SBs at the contact. It has been reported that the contact resistance is larger than the channel resistance for ultra-scaled CNTFETs [5]. This means that the contact plays a more important role than scattering in the channel for the CNTFETs with a short channel. Therefore, we suppose the carrier transport in SWNT and the Si channel is ballistic for the simplicity of calculation. This assumption may cause that the calculation result is somewhat higher than that of the actual transistors. The current is given by the Landauer-Büttiker formula.

$$I = \frac{4e}{h}\int [F(E) - F(E + eV_d)]T(E)dE, \qquad (1)$$

where V_d is the drain voltage, $F(E)$ is the Fermi function and $T(E)$ is the energy-dependent transmission through the SB between the SWNT/Si and electrodes. $T(E)$ can be estimated using the Wentzel-Kramers-

Brillouin (WKB) approximation

$$T(E) = \exp\left[-2\int_{z_1}^{z_2} k(z)dz\right], \qquad (2)$$

with the wave number

$$k(z) = \frac{2}{3aV_0}\left\{\left(\frac{E_g}{2}\right)^2 - [E + eV(z)]^2\right\}^{1/2}, \qquad (3)$$

where $a = 0.144$ nm, $E_g = 0.4\sim0.8$ eV, and $V_0 = 2.5$ eV are the C-C bond length, the SWNT band gap and the tight-binding parameter, respectively. $V(z)$ is the electrostatic potential along the channel and is obtained by numerically solving the Laplace equation. The integration is performed between the two classical turning points, z_1 and z_2 [13]. The temperature considered here is 300 K. The Fermi level, E_F, of the source and drain contacts is assumed at the middle of the SWNT band gap. It locates 0.1∼0.3 eV below the conduction band of n-Si for a Si band gap of 1.1 eV.

2 Results and Discussion

We first consider the influence of Si Fermi level (or doping level) on the transfer characteristics of the CNTFETs. For the Si Fermi level locating 0.2 eV below the conduction band ($\Delta E_{cf} = E_c - E_f = 0.2$ eV), the calculated results are shown in Fig. 2. It presents ambipolar characteristics for $V_d \geq 0.5$ V and n-type characteristics for $V_d \leq 0.25$ V. These characteristics are the same as that for the CNTFETs with Si Fermi level locating 0.3 eV below the conduction band ($\Delta E_{cf} = 0.3$ eV) [9]. The reasons for these characteristics have been discussed in detail in reference 9.

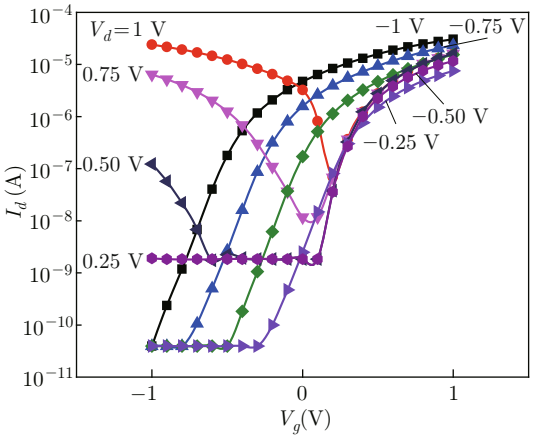

Fig. 2 Calculated transfer characteristics of the CNTFET with the Fermi level of Si locating 0.2 eV below the conduction band. The band gap of the SWNT is 0.6 eV.

Here, we focus on the differences between them. We find that both the n-branch current (at $V_g > 0$ V) and p-branch current (at $V_g < 0$ V) change with ΔE_{cf}. The minimum current points corresponding to different positive V_d also shift apparently. These can be seen much clearly in Fig. 3 which shows the transfer characteristics of the CNTFETs for three different ΔE_{cf} at $V_d = 0.75$ V. The blue, red and black curves represent $\Delta E_{cf} = 0.1$ eV, 0.2 eV and 0.3 eV, respectively. First, the n-branch current increases with decreasing ΔE_{cf} and the p-branch current decreases with decreasing ΔE_{cf}. The minimum current for $\Delta E_{cf} = 0.2$ eV is significantly higher than those for the other two cases. These phenomena can be understood using a band diagram, as shown in Fig. 4.

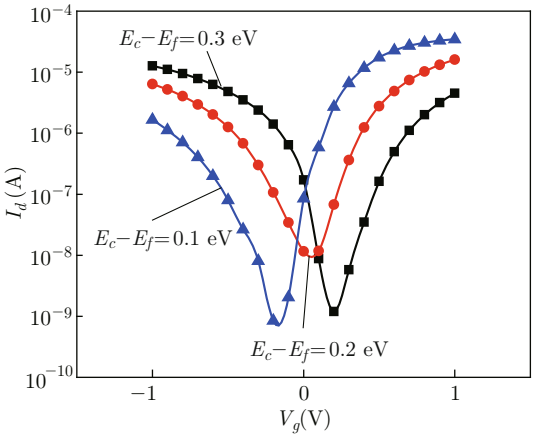

Fig. 3 Calculated transfer characteristics of the CNTFETs with different Si doping level at $V_d = 0.75$ V. The black, red and blue curves are for $E_c - E_f = 0.3$, 0.2 and 0.1 eV, respectively. The band gap of the SWNT is 0.6 eV.

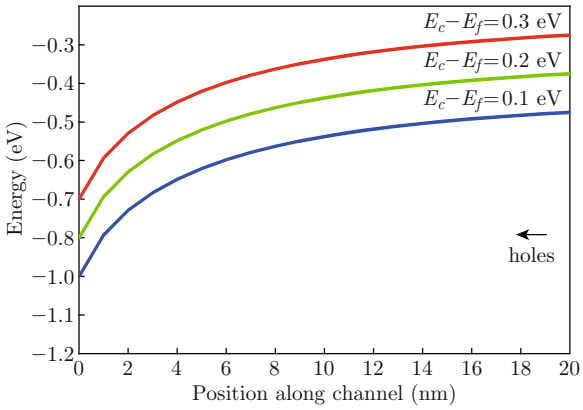

Fig. 4 Band diagrams of the CNTFETs with different Si doping level at the source side.

At a positive V_d, the band of the SWNT at the drain side bends downwards. The center channel band shifts upwards under a negative V_g, leading to a thin SB between SWNT and the drain. If it is thin enough, holes can be injected from the drain to channel, and be collected by the source, contributing to the p-branch current of the ambipolar characteristics. Since the Si band

gap (1.1 eV) is fixed, the valence band for $\Delta E_{cf} = 0.2$ eV is much lower than that for $\Delta E_{cf} = 0.3$ eV, as shown in Fig. 4. This builds a larger barrier for holes. At the same positive V_d, the lower valence band blocks more holes injected from the drain. As a result, the hole current decreases with decreasing ΔE_{cf}, as shown in Fig. 3.

The n-branch current in the ambipolar characteristics is contributed by source electrons at a positive V_d. The center channel band shifts downwards when a positive gate voltage is applied. As the increases of the gate voltage, the SB between the source and the Si becomes transparent, allowing electron injection from the source to channel. These electrons are collected by the drain, forming n-branch current. The current depends on the shape of the SB which is defined by the alignment of the Si Fermi level and the gate voltage. At the same gate voltage, the alignment of the Fermi level plays a key role in controlling the current. A smaller ΔE_{cf} means the Fermi level is much closer to the conduction band, and both the electron density and the transmission probability through the SB are higher. Therefore, the electron current increases with decreasing ΔE_{cf}, as shown in Fig. 3.

The minimum current happens at the point where the n-branch current and the p-branch current meet together. Therefore, the position of this point depends on the relative height of the two branch currents. Since the p-branch current increases with increasing ΔE_{cf} and the n-branch current decreases with increasing ΔE_{cf}, the p-branch current for $\Delta E_{cf} = 0.1$ eV is much lower than its n-branch counterpart, and hence the minimum current point is close to the p-branch part. The situation for $\Delta E_{cf} = 0.3$ eV is in contrast to that for $\Delta E_{cf} = 0.1$ eV, the minimum current point is thus on the opposite direction of the former one. The n-branch current and p-branch current for $\Delta E_{cf} = 0.2$ eV are almost symmetric with V_g, leading to a minimum current point closing to $V_g = 0$ V, and the minimum current is apparently higher than those for the other two cases.

The band gap of carbon nanotubes has important influence on the characteristics of the planar CNTFETs [19]. It is useful to know the performance of our vertical CNTFETs with different band gap. Given $\Delta E_{cf} = 0.3$ eV for Si, the transfer characteristics of the CNTFETs with different band gap are shown in Fig. 5. For the ambipolar characteristics at positive drain voltage, for example, $V_d = 1$ V, the n-branch current keeps unchanged for three different SWNT band energies, as shown in Fig. 5(a). This is because the n-branch current are contributed by the electron injection from the source, and the current depends on the SB between the source and Si. This SB does not change with the variation of the SWNT band gap. Therefore, the n-branch current are the same for the three different SWNT band gaps.

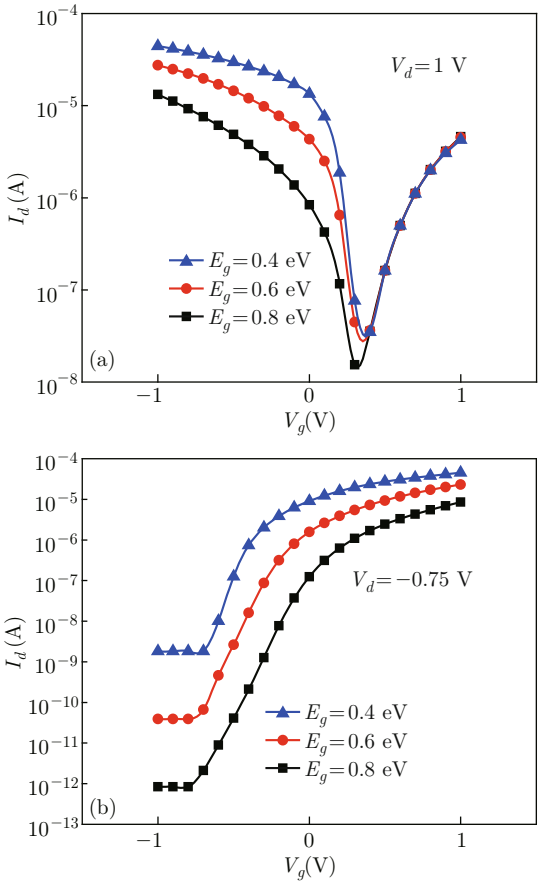

Fig. 5 Calculated transfer characteristics of the CNTFETs with different SWNT band gaps for $V_d = 1$ V (a) and $V_d = -0.75$ V (b). The blue, red, and black curves are for $E_g = 0.4$, 0.6 and 0.8 eV, respectively.

In contrast, the p-branch current in Fig. 5(a) increases with decreasing SWNT band gap. The reason is that the p-branch current is contributed by hole injection from the drain when the SWNT band bends downwards at the drain for positive V_d. The current is controlled by the SB between the SWNT and the drain. It becomes transparent for holes when a small enough V_g is applied. As the decrease of E_g, the distance between the sharp SB and the Fermi level of the SWNT decreases and both of the transmission probability and the hole density increase, leading to an increased hole current.

At a negative V_d, the SWNT band bends upwards at the drain. The electrons can be injected from the drain to the channel and form n-type current of the CNTFETs. The current depends on the shape of the SB between SWNT and the drain which define the transmission probability of the electron. This current also increases with decreasing E_g of the SWNT, as shown in Fig. 5(b). The reason is the same as that for the influence of small ΔE_{cf} on the n-branch current at a positive V_d, but the SB between SWNT and the drain instead of that between the source and Si is considered

here. As the decrease of the band gap, the Fermi level of the SWNT becomes much closer to the sharp point of the SB, resulting in a higher electron current.

We now turn to the impact of the oxide thickness on the performance of the transistors. One of the most important influences of oxide thickness is on the inverse sub-threshold slope of the CNTFETs. It is a measure of the switching speed of a transistor. The inverse sub-threshold slope is calculated using

$$S = dV_g/d(\log I_d). \quad (4)$$

It increases almost linearly from 130 to 290 mV/dec if the oxide thickness is increased from 5 nm to 25 nm, as shown in Fig. 6.

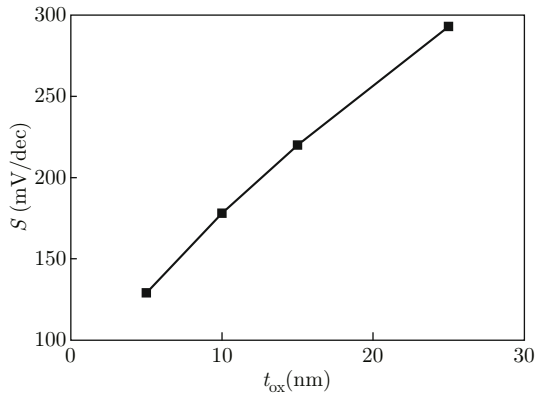

Fig. 6 Inverse sub-threshold slope as a function of the oxide thickness. The Fermi level of Si locates 0.3 eV below the conduction band. The band gap of Si and SWNT are 1.1 eV and 0.6 eV, respectively.

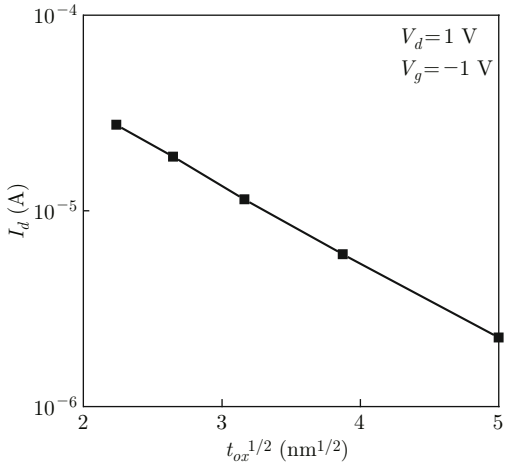

Fig. 7 Drain current as a function of square root of the oxide thickness for the CNTFETs at $V_d = 1$ V and $V_g = -1$ V.

In addition to the inverse sub-threshold slope becoming worse, the drain current also degrades significantly with increasing of the oxide thickness. Since the CNTFETs are Schottky barrier transistors, the electric field distribution in the vicinity of the contact plays a critical role in the transistor performance. This electric field distribution is significantly affected by the oxide thickness if V_g and V_d are fixed. Figure 7 shows the I_d as a function of square root of the oxide thickness at $V_d = 1$ V and $V_g = -1$ V. It can be seen clearly that I_d decreases linearly with increasing square root of the oxide thickness. The current degrades more than one order of magnitude when t_{ox} increases from 5 nm to 25 nm.

3 Conclusion

The performance of a vertical CNTFETs on n-Si was investigated using a semi-classical model. The interesting characteristics of the transistors are that can be ambipolar or unipolar depending on the sign of drain voltage. The CNTFETs show ambipolar characteristics at positive drain voltage and n-type characteristics after reversing the sign of drain voltage. The ambipolar characteristics are affected by both the Si doping level and the carbon nanotube band gap while the n-type characteristics is mainly controlled by the carbon nanotube band gap. The n-branch current for the ambipolar characteristics can be increased by increasing the Si doping level while the p-branch current can be improved by decreasing the Si doping level or decreasing the carbon nanotube band gap. In addition, the current decreases linearly with increasing square root of gate oxide thickness. It can differ by one order of magnitude if the gate oxide thickness is increased from 5 nm to 25 nm. The turn-on performance quantified by sub-threshold slope simultaneously becomes much worse. This study showed the significant basic future for designing the vertical CNTFETs on Si.

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