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Five New MVL Current Mode Differential Absolute Value Circuits Based on Carbon Nano-tube Field Effect Transistors (CNTFETs)

Mojtaba Jamalizadeh[1], Fazel Sharifi[2], Mohammad Hossein Moaiyeri[2], Keivan Navi[2,*] and Omid Hashemipour[2]

Carbon Nano-Tube Field Effect Transistors (CNTFETs) are being widely studied as possible successors to silicon MOSFETs. Using current mode has many advantages such as performing sum operation by means of a simple wired connection. Also, direction of the current can be used to exhibit the sign of digits. It is expected that the advantages of current mode approaches will become even more important with increased speed requirements and decreased supply voltage. In this paper, we present five new circuit designs for differential absolute value in current mode logic which have been simulated by CNTFET model. The considered base current for this model is 2 μA and supply voltage is 0.9 V. In all of our designs we used N-type CNTFET current mirrors which operate as truncated difference circuits. The operation of Differential Absolute Value circuit calculates the difference between two input currents and our circuit designs are operate in 8 logic levels.

Keywords: CNTFET; Current mode; Truncated difference; Differential absolute value

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The binary logic has been used in computational circuits for many decades. But, in the recent decades Multiple-Valued Logic (MVL) is considered as an alternative to the common binary logic. MVL allows more information to be transmitted over a given set of lines results in reducing complexity of interconnections, circuitry and chip area. In this logic, arithmetic operations can be executed more efficiently and faster by increasing the radix of the systems [1-4]. MVL is a mixture design techniques of binary logic and analogue signal processing which preserves noise advantages of a digital signal while processing greater information content in analogue mode.

MVL decreases parasitic related with routing and provide a higher speed of operations. There have been many efforts to derive a reasonable MVL technology based on the voltage mode. The most important obstruction to reception of any such technology is due to encoding more than two levels of logic in the available room temperature for voltage swing is decreased [5].

The possible approach to solve this problem is to use the current mode techniques that use current as a signal carrier, either alone or in combination with voltage. Recent experiences demonstrate that due to design simplicity and larger dynamic range, current mode approach is becoming attractive for the performing MVL function especially when the radix is larger than 3 and it can be also applied for higher radix MVL circuit design successfully [2,3,6]. Multi-valued current-mode circuits could be useful only if they can be implemented with today and tomorrow technologies [7].

For many years MOSFET has been used as a basic element of circuit designing. As the miniaturization of silicon based circuits reaches its physical limitations, molecular devices are becoming hopeful alternatives to the existing silicon technology

[1]Department of Computer Engineering, Science and Research Branch of Islamic Azad University, Tehran, Iran
2Faculty of Electrical and Computer Engineering, Shahid Beheshti University, GC, Tehran, Iran
*Corresponding author. E-mail: navi@sbu.ac.ir

[8,9]. Especially, unique characteristics of CNT such as high mobility of electrons, high I_{ON}/I_{OFF} ratio and their unique one dimensional band structure that suppresses back scattering and near ballistic or ballistic operation has made it as a potential successor to silicon technology[10,11]. Circuits designed based on the CNT Field Effect Transistors (CNTFETs) consume less power and are much faster than the conventional silicon FET-based circuits. Moreover, existence of same mobilities for n-type and p-type CNTFETs make the transistor sizing of the complex circuits much simpler. Moreover, CNTFETs have higher ON current than the MOSFETs for the same OFF current. Smaller molecular structure of the CNTFETs enables scaling beyond what currently available advanced lithographic techniques permit and because CNTs do not have surface dangling bonds as Silicon, some other crystalline or amorphous insulator can be used instead of SiO_2, in the structure of CNFETs. One dimensional structure of CNTs decreases the resistivity which minimizes the energy consumption. Therefore, the power consumption density in the channel of CNFET is reduced. In addition, ballistic conduction of the CNTs decreases the power dissipation in the body of CNTFETs and makes them suitable for very high speed applications. Besides the mentioned advantages of the CNFETs compared to the conventional silicon-based MOSFETs, it has also some drawbacks, such as the problems in the process of fabricating the CNFETs on currently available CMOS platform. For instance, in the integration process, local-gate CNFET is essential. However, most of the local-gate designs use metal as the gate and it is quite hard to combine the metal gate and the grown CNTs for the integration due to the metal melting point limit [12]. In addition, since carbon nanotube network films are composed of both semiconducting and metallic CNTs, CNFETs fabricated based on CNT network films may not turn off completely, which can be troublesome for integrated circuit applications. However, encouraging researches are being performed to solve these physical problems and challenges in the time to come.

Since the I-V characteristics of CNTFETs are qualitatively similar to MOSFET, most of MOS circuits can be translated to a CNTFET based design. As one of the hopeful new devices, CNTFET avoids most of the basic limitations for conventional silicon devices [8,9]. In this paper, we use single-walled carbon nanotube (SWCNT) that can be visualized as a sheet of graphite which is rolled up and joined together along a wrapping vector $C_h = n_1 \cdot \bar{a}_1 + n_2 \cdot \bar{a}_2$, where $\left[\bar{a}_1, \bar{a}_2\right]$ are lattice unit vectors , and the indices (n_1, n_2) are positive integers that identify the chirality of the tube [13]. Length of C_h is thus the circumference of the CNT, which is given by:

$$C_h = a\sqrt{n_1^2 + n_1^2 + n_1 n_2} \quad (1)$$

Single-walled CNTs are classified into one of the following three groups, depends on their chiral number (n_1, n_2): (1) armchair ($n_1 = n_2$), (2) zigzag ($n_1 = 0$ or $n_2 = 0$), and (3) Chiral (all other indices) and here we use CNT with the chiral numbers (17, 0) and (19, 0)

Carbon Nano Tube Field Effect Transistor (CNTFET)

The electrons in CNT are confined within the atomic plane of graphene. Due to the quasi-1D structure of CNT, the motion of the electrons in the nanotubes is strictly restricted. Electrons may only move freely along the tube axis direction. As a result, all wide angle scatterings are prohibited, and only forward scattering and backscattering due to electronphonon interactions, are possible for the carriers in nanotubes.

The operation principle of CNTFET is similar to that of conventional silicon devices. This three (or four) terminal device consists of a Semi-conducting Nano-tube, which is acting as conducting channel, and bridging the source and drain contacts. So, the device can be turned on or off electrostatically through the gate. The quasi-1D device structure provides better gate electrostatic control above the channel region than 3D and 2D device structures. In terms of the device operation mechanism, CNTFET can be categorized as either Schottky Barrier (SB) controlled FET (SB-CNTFET) or MOSFET-like FET [8,9].

The conductivity of SB-CNTFET is controlled by the majority carriers tunneling via the SBs at the end contacts. The on-current and consequent device performance of SB-CNTFET is determined by the contact resistance due to the existence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance. SB-CNTFET exhibits ambipolar transport behavior [11]. The work function induced barriers at the end contacts can be made to increase either electron or hole transport. Consequently both the device polarity (N-type FET or P-type FET) and the device bias point can be adjusted by choosing the proper work function of source/drain contacts. On the other hand, MOSFET like CNTFET exhibits unipolar behavior by blocking either electron (P-FET) or hole (N-FET) transport with deeply doped source/drain [14]. The non-tunneling potential barrier in the channel region, and thus

the conductivity, is modulated by the gate-source bias. Although good DC current can be achieved by SB-CNTFET with the self-aligned structure, its AC performance is going to be poor due to the nearness of the gate electrode to the source/drain metal. The ambipolar behavior of SB-CNTFET also makes it undesirable for complementary logic design. Taking into account both the fabrication achievability and higher device performance of MOSFET-like CNTFET as compared to SB-CNTFET. The CNTFET that used in HSPICE model is MOSFET-like CNTFET.

CNTFET and Current Mode Logic

In many applications, device speed is the most important requirement, and so conventional voltage mode silicon based devices cannot solve this necessity. Many years ago the current mode logic is proposed as a potential solution for this problem but combining this logic and MOSFET technology reduces the speed advantage pertains to the current mode logic, and furthermore have additional imperfection due to using MOSFET technology. In recent years, this technology has been entered in nano scale region as continues to scale deeper into the nanoscale, device non idealities cause I-V characteristics to be substantially different from well tempered MOSFETs that increase the deficiencies of using silicon based technology.

In the last few years, the research on nanotechnology has been increased particularly on the nanoelectronics. Carbon Nano-tube (CNT) technology is at the front of these technologies due to the unique mechanical and electronic properties [15,16]. Using this technology can reduce the most of the imperfections of silicon based technology. There are three reasons why CNTFET is the most hopeful technology to expand or complement conventional silicon technology: Firstly, the operation principle and the device structure are as the same as MOSFET devices; we can use again the conventional MOSFET based design infrastructure. Secondly, we can use again MOSFET fabrication method. Thirdly, the best experimentally demonstrated CNTFET device shows very good current carrying ability. By employing this technology the device speed will be improved. However, utilizing CNTFET together with current mode logic style leads to a remarkable increase of device speed.

Five New MVL Current Mode Differential Absolute Value Circuits Based On Carbon Nano-tube Field Effect Transistors

In the following designs, we used N-type CNTFET current mirrors which act as truncated difference. The main component of all these designs is the truncated difference and its operation is defined as follows:

$$In1 \ominus k * In2 = \begin{cases} Z = In1 - k * In2 & if\ (In1 \geq k * In2) \\ Z = 0 & otherwise \end{cases} \quad (2)$$

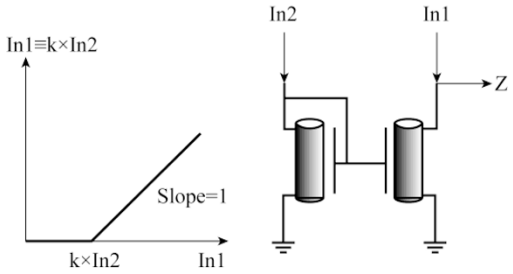

FIG. 1. Circuit design of truncated difference.

The circuit design of truncated difference is showed in Fig.1.

In some of these designs we used N-type CNTFETs for unidirectional current to the output and P-type CNTFET current mirrors due to inversing the current direction to achieve the appropriate current output direction. These circuits exhibit the arithmetic operation |input1-input2|. Input1 and input2 are the main inputs of our designs. If input1<input2 then the output will be equal to “input2-input1” else we will have “input1-input2” at the output node. The Z1 and Z2 are connected to Z which describes our final output. In our simulation results we apply 10

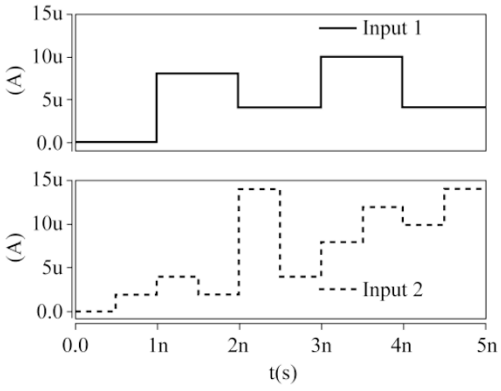

FIG. 2. Inputs of our circuits in transient simulation.

μA as the highest current level in input1 and we will have 14 μA as the highest current level for the second input (Fig.2).

Design 1

Four CNTFET current mirrors have been used in this design which three of them are N-type and the other one is P-type. By using M7 we will have the copy of drain current of M3. This circuit has two input, and also we used a copy of them in our design. In this design Z1 is connected to the drain node of M6 and Z2 is connected to the source node of M9.

When input1<input2, M1 and M2 will be turned on and base on KCL law the drain current of M3 is equal to zero, hence base on current law the M4 and M7 will be cut off, i.e. their drain current are equal to 0. The drain current of M5 is equal to input1 and the drain current of M6 is equal to input1 (current mirror) and therefore the output Z1 is "input2-input1". When M7 is cut-off then M8 and M9 will be cut-off and we haven't any current in Z2 and finally the output is equal to "input2-input1".

When input2<=input1, M1 and M2 will be turned on and base on KCL law the drain current of M3 is equal to "input1-input2", therefore the drain current of M4 is equal to "input1-input2". Base on KCL law the drain current of M5 is equal to "input2" and the drain current of M6 is the same as previous (equal to "input2") so that Z1 is equal to 0. The drain current of M7 is equal to "input1-input2" and the P-type current mirror will inverse the current direction and the output Z2 and thereby the circuit output will be equal to "input1-input2" (Fig. 3& Fig. 4).

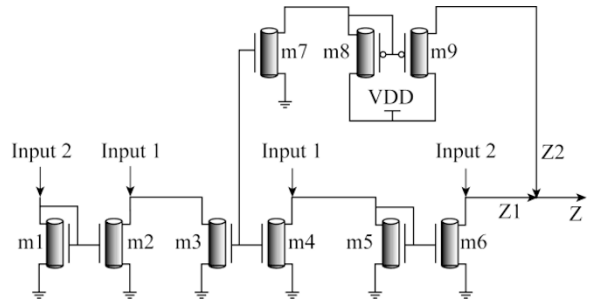

FIG. 3. Design 1 Z=|input1-input2|.

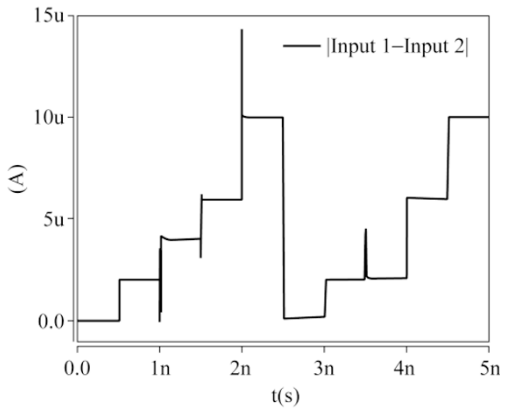

FIG. 4. Transient simulation result of design 1.

Design 2

In this design we used one P-type CNTFET current mirror for inversing the current direction, and by connecting the gates of M2 and M5, we have two copies of drain current of M1 in drains of M2 and M5 which act as truncated and one N-type CNTFET which its drain and its gate are connected to each other and its duty is unidirectional current from drain node of M5 to the output. This circuit has two inputs that in this design we need a copy of one of them too. In this design the currents of Z1 and Z2 come from the source node of M6 and the drain node of M4.

When input1<input2, M1, M2 and M5 are turn on and base on KCL law and truncated difference the current equal to "input2-input1" comes from M2 and M5 drain nodes and enter to the drain nodes of M3 (upper section) and M6 (lower section) respectively but M3 and therefore M4 are cut-off (P-type current mirror) and hence the upper path is cut-off too and Z2 is equal to 0. In lower path the current equal to "input2-input1" that comes from drain node of M5 can pass through M6, so that Z1 is equal to "input2-input1" and finally the circuit output will be equal to "input2-input1".

When input2 ≤ input1, M1, M2 and M5 will be turn on and in this situation M6 is cut-off and the drain current of M6 is equal to 0, therefore the lower pass is cut-off too and we haven't any current in Z1, and base on KCL law and truncated difference the current equal to "input1-input2"enter to the drain node of M2 and the P-type current mirror will inverse the current direction to the output Z2 and thereby the circuit output will be equal to "input1-input2".

In this design the existence of M6 is important, because if we eliminate this transistor and replace it by a wire when input2 ≤ input1 the lower path will be open and a current can enter to the drain node of M5, hence the output current will reduce and our circuit will not work properly (Fig. 5 and Fig. 6).

Design 3

In this design we have two truncated difference circuits and two P-type current. This circuit has two inputs and a copy of them. The currents of Z1 and Z2 exit from the drains of M8 and M4 respectively. The function of this design is very simple.

When input1<input2, M1, M2, M5, M6 will be turn on and base on KCL law and truncated difference and current mirror there is no current in the drain of M3, therefore M3 and M4 are cut-off and we have no any current in Z2 and in this time in the

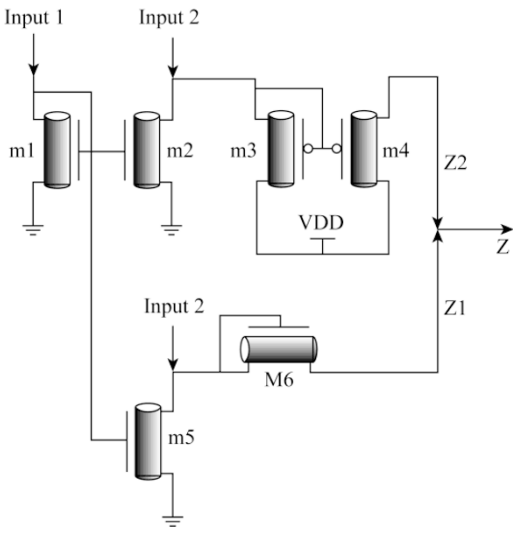

FIG. 5. Design 2 Z=|input1-input2|.

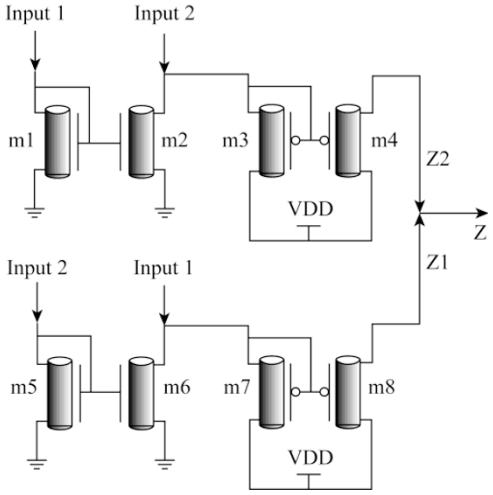

FIG. 7. Design 3 Z=|input1-input2|.

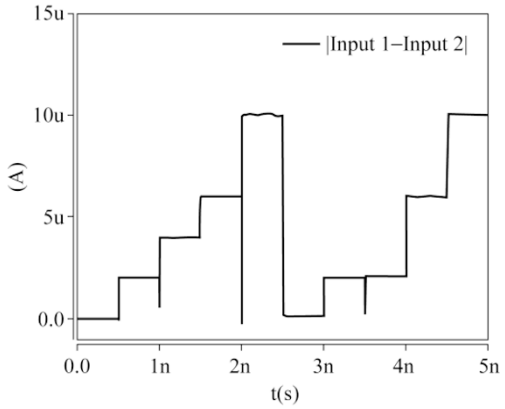

FIG. 6. Transient simulation result of design 2.

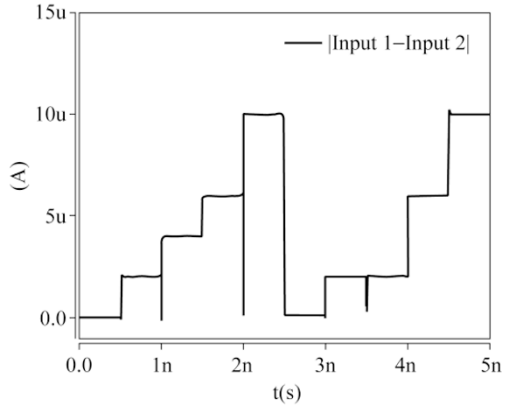

FIG. 8. Transient simulation result of design 3.

lower section of this circuit the current equal to |input2-input1| will enter to the drain node of M6 and the P-type current mirror will inverse the direction of this current to the output Z1 and we will have the current equal to "input2-input1" in the output of our circuit.

When input2 ≤ input1, the function in the upper and lower sections of this circuit design will swap and the output of circuit will be equal to "input1-input2" (Fig. 7, Fig. 8).

Design 4

Two N-type CNTFET current mirrors which operate as truncated difference and two N-type CNTFET that in each one their gates and drains are connected to each other and conduct a unidirectional current from drain nodes of M2 and M5 to the output are the components of this circuit design. This circuit has two inputs and a copy of each one and the currents of Z1 and Z2 exit from the sources of M6 and M3 respectively.

When input1<input2, M1, M2, M4 and M5 are turn on and base on KCL law and truncated difference the current equal to "input2-input1" exit from the drain node of M2 and thereby the M3 will be turn on and can conduct this current to the output, therefore the current of Z2 is equal to "input2-input1". And in the lower section of this circuit there is no current in the drain of M6 and thereby in the output Z1. Finally the sum of Z1 and Z2 which is the circuit output is equal to "input2-input1".

When input2<=input1, the operations of upper and lower section of this design will swap, i.e. Z1 and Z2 will be equal to "input1-input2" and "0" respectively and therefore the circuit output will be equal to "input1-input2" (Fig. 9, Fig. 10).

Design 5

One N-type CNTFET truncated difference and one P-type CNTFET current mirror and one N-type CNTFET that its drain and its gate are connected to each other for the unidirectional

current from the drain node of M2 to the output has been used. This circuit has two inputs, and Z1 and Z2 are connected to the source of M3 and to the drain of M5 respectively and their current will be sum at the output node and the result of this sum is the output of the circuit.

When input1<input2, M1 and M2 will be turned on and base on KCL law and truncated difference the current equal to "input2-input1" exit from the drain node of M2 and thereby M4 and M3 will be cut-off and turn on respectively, therefore the M5 which its gate is connected to the gate and drain of M4 will be cut-off too, hence we haven't any current in the output Z2. In this time the current equal to "input2-input1" will pass through M3, therefore output Z1 and thereby the output of our circuit will be equal to "input2-input1".

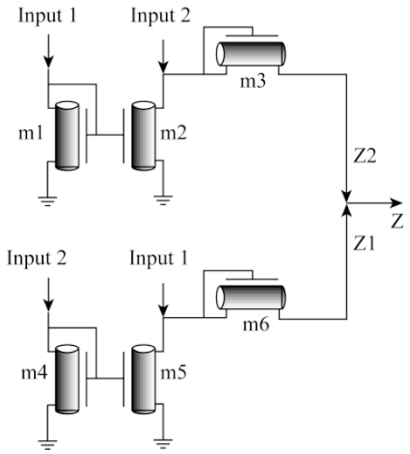

FIG. 9. Design 4 Z=|input1-input2|.

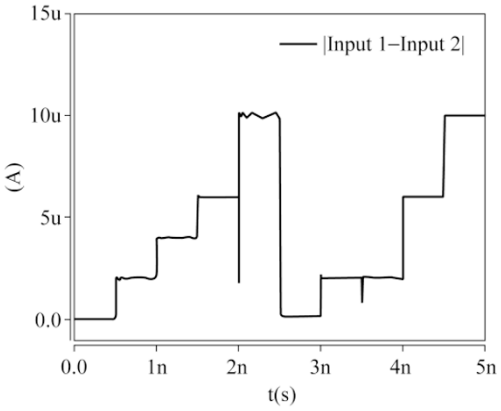

FIG. 10. Transient simulation result of design 4.

When input2<=input1, M1 and M2 will be turn on and the current equal to "input1-input2" enter to the drain node of M2, hence we have no current in the drain of M3 and consequently it will be cut-off, therefore output Z1 is equal to "0". In this situation P-type current mirror will inverse the current direction and the current equal to "input1-input2" will be at the output Z2 and thereby at output of our circuit.

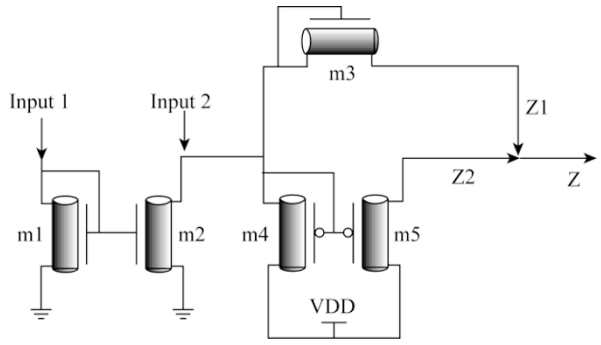

FIG. 11. Design 5 Z=|input1-input2|.

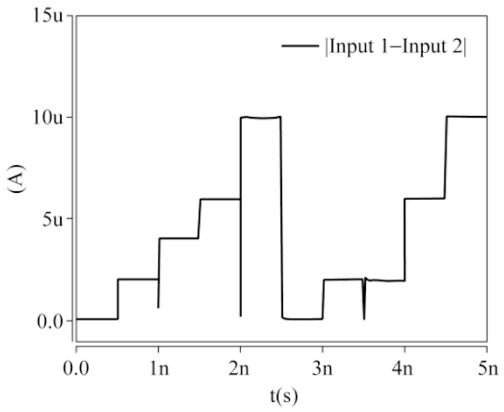

FIG. 12. Transient simulation result of design 5.

In this design the role of M3 is important. If we eliminate this transistor and replace it by a wire when input2<=input1 we will face with some problems: In some amount of inputs either some of drain current of M5 which must enter the output completely maybe enter the M2 drain node and proper output will be reduced and changed, or some of drain current of M4 that must enter to the drain node of M2 completely maybe enter the output and the output will be increase, in these situations we will not have proper output in our circuit output. We reduced the diameter of transistor M3 by changing the chiral number to (n1=9, n2=0) and thereby the threshold voltage of this transistor has been raised, because when the current comes from M4 drain and must enter to the M2 drain completely, some of this current can pass through M3 and enter the output which rise and change the proper output that rising threshold voltage of transistor M3 can solve this problem (Fig. 11, Fig. 12).

Simulation Results

In this paper we have used Carbon-nanotube Field Effect Transistors SPICE Model which is implemented based on "A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors" [8,9,17]. This

Table 1. CNFET model parameters

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20 pF/m
Efi	The Fermi level of the doped S/D tube	6 eV

standard model has been designed for unipolar, MOSFET-like CNFET devices, in which each transistor may have one or more CNTs. In this model we also considered Schottky Barrier Effects, Parasitics, including CNT, Source/Drain, and Gate resistances and capacitances, and CNT Charge Screening Effects. The parameters of the CNFET model and their values, with brief descriptions, are shown in Table 1. All of the simulations have been done at room temperature at 0.5 V and 0.65 V supply voltages. We have used 0.9 V supply voltage for this CNTFET circuit and the delay, power consumption and PDP [18] have been measured using HSPICE. This model is designed for unipolar behavior MOSFET-like CNTFET device. The minimum channel length (~10 nm) is confined by the complex quantum mechanisms which are not implemented in this model. This model has no limitation on the maximum gate length of CNTFET.

For gate length longer than 100 nm, the device is treated as long channel device. The transition from the short channel model (10 nm $\leq$ Lg $\leq$ 100 nm) to the long channel model (Lg > 100 nm) is continuous and is automatically handled by the model [8,9].

The CNTFET on-current can be approximated as:

$$I_{\mathrm{CNTFET}} = \frac{n \cdot \mathrm{g_{CNT}} \left(\mathrm{V_{DD}} - V_{th,CNT} \right)}{1 + \mathrm{g_{CNT}} L_S \rho_S} \tag{3}$$

The parameter n is the number of CNTs per device, $V_{th,CNT}$ is the threshold voltage and is about 0.3V for chirality (19, 0) semi-conducting CNT, g_{CNT} is the transconductance per CNT, and L_s is the source length (doped CNT region), and ρ_s is the source resistance per unit length of doped CNT. CNTFET device delay CV/I can be shown as:

$$\tau_{CNTFET} = \eta_{CNT,C} \cdot \eta_{CNT,R} \cdot \frac{C_{gc,CNT} L_g V_{DD}}{g_{CNT} \left(V_{DD} - V_{th,\mathrm{CNT}} \right)} \tag{4}$$

The gate to channel capacitance $C_{gc,CNT}$ is the capacitance per unit CNT length [8,9]. We define the pre-factor η_{CNT} as:

$$\eta_{CNT} = \eta_{CNT,C} \cdot \eta_{CNT,R} \tag{5}$$

$$\eta_{CNT,C} = \left(1 + \frac{\mathrm{C_{gtg}} W_g}{n \cdot \mathrm{C_{gc,CNT}} L_g} \right) \tag{6}$$

$$\eta_{CNT,R} = \left(1 + \mathrm{g_{CNT}} L_S \rho_S \right) \tag{7}$$

C_{gtg} is the gate parasitic coupling capacitance connected between the gate and the source/drain/ground or the gate of the adjacent devices, according to the device layout. Therefore the CNTFET device intrinsic speed is degraded by both the pre-factor $\eta_{CNT,C}$ due to the gate parasitic capacitance and the pre-factor $\eta_{CNT,R}$ due to the extension series resistance. Compared to silicon technology, CNTFET show much better

Table 2. Comparison simulation results of five circuit designs of differential absolute value in CNTFET model

PDP (J)	Delay (s)	Power (W)	Proposed Designs
3.1681E-16	1.688E-11	2.9643E-05	Desgin 1
2.3790E-16	1.2415E-11	1.9162E-05	Desgin 2
5.6610E-16	1.8014E-11	3.1425E-05	Desgin 3
2.8883E-16	1.0440E-11	2.7665E-05	Desgin 4
1.4102E-16	1.0714E-11	1.3162E-05	Desgin 5

device performance based on the intrinsic CV/I gate delay metric (6 for N-FET and 14 for P-FET) than MOSFET device at the 32 nm node, even with device non-idealities. This large speed improvement is significantly degraded (by a factor of 5 to 8) by interconnect capacitance in a real circuit environment [8,9].

Due to the transistor sizing and the set chiral numbers for the CNTs, i.e. (17,0) for P-FETs and (19,0) for N-FETs, to make the circuits operate correctly, the N-FETs operate faster than the P-FETs, in the proposed circuits. Therefore, in spite of using 9 transistors in design 1, this design has lower power consumption and delay rather than design3 which has been used 8 transistors. This is due to the fact that in design3 four P-type transistors are used whereas in design1 two P-type transistors are used. Design4 has lower delay and power consumption compared to design1 because less number of transistors (6 transistors) is used in that design and also the critical path of design1 is longer. Design4 has two copies of each input whereas design2 has two copies of one of the inputs and one copy of the other one. This cause more current flowing in design4, which brings about more power consumption of design4 compared to Design2. Because of using two P-type transistors in design2, this design has more delay than design4. Design5 has the lowest power consumption considering the proposed designs because this design has just 5 transistors and no extra copies of the inputs. However, this design has more delay in comparison with design4 because two P-type transistors have been used in design5.

Conclusion

In this paper we presented five designs of MVL current mode Differential Absolute Value circuit, based on Carbon Nano-tube Field Effect Transistors. These circuits take advantages of current mode and MVL. To evaluate their performance, circuits have been simulated on HSPICE by using a CNTFET compact model for CNTFET.

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