NANO-MICRO LETTERS ARTICLE
www.nmletters.org

Comparative Performance Evaluation of Large FPGAs with CNFET- and CMOS-based Switches in Nanoscale

Mohammad Hossein Moaiyeri[a,b], Ali Jahanian[a,c], Keivan Navi[a,b,*]

(Received 17 July 2011; accepted 21 September 2011; published online 27 September 2011.)

Abstract: Routing resources are the major bottlenecks in improving the performance and power consumption of the current FPGAs. Recently reported researches have shown that carbon nanotube field effect transistors (CNFETs) have considerable potentials for improving the delay and power consumption of the modern FPGAs. In this paper, hybrid CNFET-CMOS architecture is presented for FPGAs and then this architecture is evaluated to be used in modern FPGAs. In addition, we have designed and parameterized the CNFET-based FPGA switches and calibrated them for being utilized in FPGAs at 45 nm, 22 nm and 16 nm technology nodes. Simulation results show that the CNFET-based FPGA switches improve the current FPGAs in terms of performance, power consumption and immunity to process and temperature variations. Simulation results and analyses also demonstrate that the performance of the FPGAs is improved about 30%, on average and the average and leakage power consumptions are reduced more than 6% and 98% respectively when the CNFET switches are used instead of MOSFET FPGA switches. Moreover, this technique leads to more than 20.31% smaller area. It is worth mentioning that the advantages of CNFET-based FPGAs are more considerable when the size of FPGAs grows and also when the technology node becomes smaller.
Keywords: Carbon nanotube field effect transistor (CNFET); FPGA switches; Performance evaluation; Power consumption; Process variation

Citation: Mohammad Hossein Moaiyeri, Ali Jahanian and Keivan Navi, "Comparative Performance Evaluation of Large FPGAs with CNFET- and CMOS-based Switches in Nanoscale", Nano-Micro Lett. 3 (3), 178-188 (2011). http://dx.doi.org/10.3786/nml.v3i3.p178-188

Introduction

Current FPGAs contain many resources consisting logic blocks, interconnect switches, SRAM cells, variety of hard coded blocks, and even some full processors. However, interconnects are the major concern in new FPGAs. The interconnect switch resources in Xilinx's Virtex-II FPGAs take around 70% of the CLB area. Furthermore, even after careful timing-driven packing and placement, interconnects are the dominant source of delay for most designs and more than 80% of the total critical path delay is due to interconnect resources. In addition, the power consumption in a typical FPGA mapped design is dominated (more than 70%) by the interconnect resources [1]. In this situation, improving the properties of the interconnect switches has a considerable impact on the characteristics of FPGAs. Delay and power consumption of the switches can be reduced considerably by using Carbon nanotube field effect transistors (CNFETs). In general, CNFET has higher performance and lower power consumption compared to silicon-based MOSFET [2] and is very appropriate for low-voltage applications. In addition, serious challenges of CMOS technology such as

[a]Faculty of Electrical and Computer Engineering. Shahid Beheshti University, G.C., Tehran, Iran
[b]Nanotechnology and Quantum Computing Lab. Shahid Beheshti University G. C., Tehran, Iran
[c]VLSI Design Automation Lab. Shahid Beheshti University G. C., Tehran, Iran
*Corresponding author. E-mail: navi@sbu.ac.ir

large parametric variation, reduced gate control, short-channel effects, very high leakage currents and high power densities, makes the scientists and researchers eager to work toward the new nanotechnologies such as quantum-dot cellular automata [3] and CNFETs [4-6] as the possible successors to the conventional silicon-based MOSFET technology. Moreover, due to the similarities between MOSFETs and CNFETs in terms of intrinsic characteristics and operation, CNFET seems to be more feasible and promising, compared to the other emerging nanotechnologies. In Ref. [7], the CAD implications of possible new interconnect technologies have been reviewed. Authors of Ref. [7] considered three technologies in particular: three dimensional ICs, carbon nanotubes (CNTs) and RF/optical interconnections for longer range on-chip communication. In Ref. [8], a brief overview of CNFET technology has been presented and commonly raised concerns through a series of Frequently Asked Questions (FAQs) about carbon nanotubes have been addressed. Authors of Ref. [8] have provided a CNFET technology outlook, which includes a survey of challenges as well as existing and potential solutions to these challenges. They have explained the main questions about the carbon nanotube technology. They have described that carbon nanotubes can be integrated with silicon MOSFET, as CNFETs [8]. In Ref. [10], a carbon nanotube based FPGA architecture has been proposed in which, lookup tables are implemented using carbon nanotube transistors but FPGA routing resources are designed by nano-switch devices. In Ref. [11] a new architecture for FPGA interconnect utilizing bundles of single-walled carbon nanotubes (SWCNT) has been presented and the gained performance has been compared with the standard copper interconnects. The results of Ref. [11] demonstrates that FPGAs, utilizing SWCNT bundle interconnects, can achieve about 19% improvement in average area delay product over the best performing architecture for standard copper interconnect at 22 nm process technology. In Ref. [12], a novel high performance reconfigurable architecture, called NATURE has been proposed that utilizes CMOS logic and nanotube-based RAMs.

As described, in the mentioned contributions, using the carbon nanotubes have been evaluated in CLB transistors and also in FPGA wires. However, implementing the FPGA interconnect switches with CNFETs, which significantly affects the performance of the whole FPGA, has not been investigated.

In this paper, we adjust the basic parameters of CNFETs for using in modern FPGA technologies. Afterwards, we evaluate the advantages of using these transistors in FPGAs. Finally, the performance, power consumption, area and sensitivity of the resulting switches and FPGAs to the process variations are evaluated. Our analyses show that the electrical and physical characteristics of FPGAs can be improved considerably by utilizing the CNFET-based switches.

The rest of this paper is organized as follows: section 2 reviews the carbon nanotube technology and in section 3, the proposed hybrid CMOS-CNFET FPGA architecture is described. Experimental results and analyses are reported in section 4 and finally, section 5 concludes the paper.

Carbon Nanotube Field Effect Transistors (CNFETs)

A carbon nanotube (CNT) is a rolled up sheet of graphite which can be single-wall carbon nanotube (SWCNT) or multi-wall carbon nanotube. An SWCNT is composed of one cylinder and a multi-wall carbon nanotube (MWCNT) has more than one cylinder. An SWCNT can be metallic or semiconducting based on its Chiral vector determined by (n_1, n_2) indices [13]. The Chiral vector determines the arrangement angle of the carbon atoms along the carbon nanotube. If $n_1 - n_2 = 3k$ $(k \in \mathbb{Z})$, the SWCNT is metallic and otherwise it is semiconducting [14]. In CNFET semiconducting SWCNTs are utilized as the channel of the transistor. A CNFET may have one or more SWCNTs as its channel. The distance between the centers of two adjacent CNTs under the same gate is called Pitch. It directly affects the width of the gate and contacts of the CNFET. The width of the gate of a CNFET can be calculated by the following equation [15]:

$$W_{\mathrm{g}} = Min(W_{\min}, (N-1)\,\mathrm{Pitch} + D_{\mathrm{CNT}}) \qquad (1)$$

Where $W_{\min}$ is the minimum width of the gate and N is the number of adjacent SWCNTs beneath the gate. A significant attribute of CNFETs is that P-CNFET and N-CNFET have the same motilities ($\mu_{\mathrm{n}} = \mu_{\mathrm{p}}$) which is very important for transistor sizing of complex circuits [2]. Another important property of the CNFET device is that its I-V characteristic is similar to a well-tempered MOSFET device. In addition, a CNFET has also threshold voltage which is required to turn on the device electrostatically via the gate.

One of the great advantages of the CNFET compared to MOSFET is that the threshold voltage of the CNFET is adjustable by regulating the diameter of its nanotubes which makes it more flexible than MOSFET for designing digital circuits. The threshold voltage of a CNFET is nearly considered as the half band gap and can be calculated by the following equation [15]:

$$V_{\mathrm{th}} \approx \frac{E_{\mathrm{g}}}{2e} = \frac{\sqrt{3}}{3}\frac{aV_{\pi}}{eD_{\mathrm{CNT}}} \approx \frac{0.436}{D_{\mathrm{CNT}}(\mathrm{nm})} \qquad (2)$$

Where parameter $a(\approx 2.49\,\mathrm{nm})$ is the carbon to carbon atom distance, V_{π} $(\approx 3.033\,\mathrm{eV})$ is the carbon $\pi - \pi$ bond

energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the diameter of CNT. It can be inferred from Eq. 2 that the threshold voltage of the CNFET is an inverse proportion function of the carbon nanotube diameter, which is given by the following equation [15]:

$$D_{\mathrm{CNT}} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \approx 0.0783\sqrt{n_1^2 + n_1 n_2 + n_2^2} \quad (3)$$

The gate capacitance of a CNFET (C_{g}), which considerably affects the performance of the device, is composed of three components [15,16]; gate to channel capacitance ($C_{\mathrm{gc\_tot}}$), gate outer fringe capacitance ($C_{\mathrm{fr\_tot}}$) and coupling capacitance between the gate and the adjacent contacts ($C_{\mathrm{gtg\_tot}}$). Gate to channel capacitance of the CNFET device is composed of two components, $C_{\mathrm{gc\_e}}$ and $C_{\mathrm{gc\_m}}$, which are the capacitances of the CNTs located in the edge and middle of the CNFET device, respectively. Figure 1 shows the components of the gate to channel capacitance of the CNFET device.

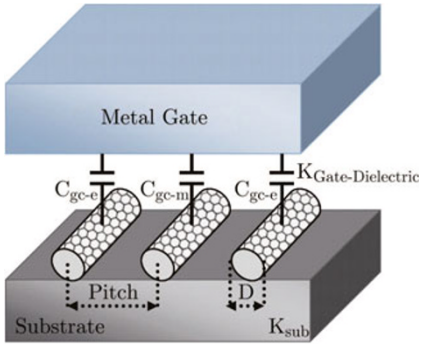

Fig. 1 The gate to channel capacitance.

Gate to channel capacitance per unit CNT length (C_{gc}) can be calculated for N carbon nanotubes under the same gate by the following equation, based on these two parameters ($C_{\mathrm{gc\_e}}$ and $C_{\mathrm{gc\_m}}$):

$$C_{\mathrm{gc}} = \mathrm{Min}(N, 2)C_{\mathrm{gc\_e}} + \mathrm{Max}(N-2, 0)C_{\mathrm{gc\_m}} \quad (4)$$

The parameters of the total gate capacitance of the CNFET device can be calculated by the following equations:

$$C_{\mathrm{gc\_tot}} = C_{\mathrm{gc}} L_{\mathrm{g}} \quad (5)$$

$$C_{\mathrm{fr\_tot}} \approx C_{\mathrm{fr}} L_{\mathrm{s}} \quad (6)$$

$$C_{\mathrm{gtg\_tot}} = C_{\mathrm{gtg}} W_{\mathrm{g}} \quad (7)$$

Where, L_{g} and W_{g} are the channel length and channel width of CNFETs respectively and L_{s} is the length of doped source side extension region. C_{fr} is the gate outer fringe capacitance per unit CNT length, and C_{gtg} is the gate coupling capacitance per unit gate width. It is notable that C_{fr} can be ignored because its value is normally quite smaller than C_{gc} and C_{gtg} [15]. As a result, total gate capacitance can be approximated as follows:

$$C_{\mathrm{g}} \approx C_{\mathrm{gc\_tot}} + C_{\mathrm{gtg\_tot}} \approx C_{\mathrm{gc}} \mathrm{L_g} + C_{\mathrm{gtg}} W_{\mathrm{g}} \quad (8)$$

In addition, the source/drain capacitance of a CNFET ($C_{\mathrm{s/d}}$) can be almost given by the following equation:

$$C_{\mathrm{s/d}} = C_{\mathrm{gs/gd}} \left(1 + \frac{C_{\mathrm{sub}}}{C_{\mathrm{ox}}}\right) \quad (9)$$

Where C_{ox} is the capacitance between the gate and channel, C_{sub} is the capacitance between the channel and the substrate and $C_{\mathrm{gs/gd}}$ is the capacitance of the gate to the source/drain contact. It is worth mentioning that $\frac{C_{\mathrm{sub}}}{C_{\mathrm{ox}}}$ is only important when the substrate is the driving (switching) gate [17].

Three different kinds of CNFETs have been presented so far which are Schottky Barrier CNFET (SB-CNFET) (Fig. 2(a)), MOSFET-like CNFET (Fig. 2(b)) and tunneling CNFET (T-CNFET) (Fig. 2(c)) [21-24]. However, considering these types of CNFETs, we have chosen MOSFET-like CNFET for our application due to its suitability for designing CMOS-based architectures, likeness with MOSFET in terms inherent electrical characteristics and device structure and ultra high performance.

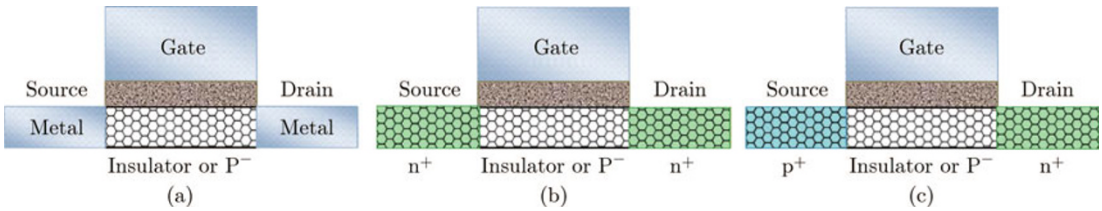

Fig. 2 Three different types of the CNFET devices (a) SB-CNFET (b) MOSFET-like CNFET (c) T-CNFET.

The Proposed Hybrid FPGA Architecture

Recently reported researches have proven the feasibility of fabricating the carbon nanotubes on a silicon wafer. In Ref. [18], a method has been proposed for fabricating the MWCNTs with diameters ranging from 30 nm to 80 nm on CMOS wafers with 100% yield. Authors of Ref. [19] reported the fabrication of an integrated circuit with silicon-based transistors and CNT

interconnects operating above 1 GHz. They assembled MWCNT interconnects on the top of a CMOS chip containing about 11000 transistors in 0.25 μm technology.

A hybrid FPGA architecture, based on MOS and CNT transistors, is presented in this paper to evaluate the proposed idea. In this architecture, CLBs and SRAM cells are implemented by MOS transistors and the FPGA wires are fabricated with metal whereas the FPGA interconnect switches are designed with CNFETs. This architecture is called CNPGA in this paper. Considerable researches have been reported on separating the routing resources in many modern FPGA technologies, especially in three-dimensional chips [20]. CNFET-based routing switches in the proposed architecture may be fabricated on a CMOS wafer or can be constructed as an auxiliary layer in a three-dimensional chip. In this architecture, all of the conventional assumptions about FPGAs are remained unchanged and the routing switches are changed. We design and parameterize the various types of FPGA switches with CNFETs to be used efficiently. A considerable part of the contributions of this paper is focused on the designing, customizing and comparative evaluating of the CMOS- and CNFET-based switches for utilizing in the large FPGAs. Afterwards, the impacts of the designed CNFET-based switches are evaluated in FPGAs.

Simulation Results

In this section the performance, power consumption and other basic features of the proposed FPGA architecture and switches are evaluated and compared with the ordinary MOSFET-based FPGAs. We have used Versatile Place and Route (VPR) tool [25] to investigate the benefits of CNFET-based FPGAs in a standard design flow. Original VPR tool is responsible for FPGA placement and routing but it has no power analyzer. PowerModel [26] is an extended version of VPR that performs power estimation for FPGAs corresponding with the normal operation of conventional VPR. Therefore, we have employed the PowerModel to evaluate the improvement of CNFET-based FPGAs compared to the conventional MOSFET-based FPGAs. The main inputs of the PowerModel tool are architecture and design files. Architecture files describe the structure and electrical characteristics of the FPGA including logic blocks, IO pins, and interconnect switches. Input design files consist of the netlist of the designs. Microelectronics Center of North Carolina (MCNC) benchmarks [27] have been used for testing the proposed architecture. MCNC comprises industrial and academic logic synthesis and optimization benchmark sets. These benchmarks contain standardized libraries with simple and advanced circuits acquired from industry. The MCNC circuits are utilized to examine all aspects of FPGA architecture such as logic block type and routing architecture. It is worth mentioning that these benchmarks are very common in scholarly research.

The 4x4LUT is utilized as the original architecture and two versions of the 4x4LUT architecture file are generated to compare the proposed architecture with the ordinary FPGAs. The first architecture file contains the parameters of the MOSFET-based FPGA switches and the second file includes the parameters of the CNFET-based FPGA switches. Both files are generated for 45 nm, 22 nm and 16 nm technology nodes. Afterwards, all of the benchmarks are evaluated by PowerModel using both architecture files and the results are compared and analyzed. We have used the netlist files of MCNC benchmarks in *.blif* format, remapped them and generated mapped netlist in *.net* file format corresponding with the stochastic signal activities by TV-pack. Finally, this information is fed into PowerModel for power/delay measurement. The utilized FPGA architecture has two types of switches: pass-transistors (PT) and tri-state buffers (TB). A tri-state buffer switch is used as an output buffer to drive tri-state buffer switched wires and also as a tri-state buffer within the routing. In addition, in this architecture conventional buffers are used at the output of the CLBs to drive the pass-transistor switched wires and to restore the voltage levels. An architecture file also contains the parameters of the switches, including resistance (R), input capacitance (C_{in}), output capacitance (C_{out}) and the intrinsic delay of the switches (T_{del}). These parameters are obtained for both MOSFET and CNFET switches at 45 nm, 22 nm and 16 nm technology nodes. Detailed parameters of the switches are calibrated using Synopsys HSPICE 2007 simulator with standard CMOS technologies and the compact SPICE model for CNFETs including non-idealities [17,28]. This standard model has been designed for unipolar enhancement-mode MOSFET-like CNFET devices, which operates correctly for CNFETs with the minimum channel length of 10 nm. In this model each CNFET may include one or more CNTs as its channel. This model also considers a realistic, circuit-compatible CNFET structure and includes practical device nonidealities, parasitics, Schottky-barrier effects at the contacts, inter-CNT charge screening effects, doped source-drain extension regions, scattering (nonideal near-ballistic transport), back-gate (substrate bias) effect and Source/Drain, and Gate resistances and capacitances. The model also includes a full transcapacitance network for more accurate transient and dynamic performance simulations. The parameters of the CNTFET model and their values, with brief descriptions, are shown in Table 1.

The values of the capacitors in the MOSFET-based switch are obtained from the HSPICE output and the values of the capacitors of the CNFET-based switches

are calculated using the mentioned HSPICE model, mainly based on Eq. 8 and Eq. 9. Moreover, the resistance of the switches is obtained according to their I-V characteristic curves. In addition, the propagation delay (T_{del}) of the switches is measured at 0.9 V supply voltage at room temperature. The tri-state buffer switches, including a buffer and a pass-transistor, are demonstrated in Fig. 3 for CMOS and CNFET technologies. The switches are sized properly, in order to reach the highest performance and driving capability. The values of the basic parameters for the switches are shown in Table 2 and Table 3. In the following sub-sections, the characteristics of the designed CNFET-based switches are evaluated and compared with the conventional MOSFET-based switches and the advantages of using the CNFET switches in FPGAs are evaluated.

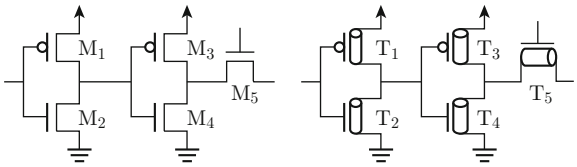

Fig. 3 CMOS and CNFET tri-state buffer switches.

Table 1 CNTFET Model Parameters.

Parameter	Description	Value
L_{ch}	Physical channel length	$\geq$ 10 nm
L_{geff}	The Scattering mean free path in the intrinsic CNT channel and S/D regions	100 nm
L_{ss}	The length of doped CNT source-side extension region	$\geq$ 10 nm
L_{dd}	The length of doped CNT drain-side extension region	$\geq$ 10 nm
K_{ox}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material (HfO_2)	4 nm
K_{sub}	The dielectric constant of substrate (SiO_2)	4
C_{sub}	The coupling capacitance between the channel region and the substrate (SiO_2)	20 aF/μm

Table 2 Basic parameters of the used CNFET switches.

Feature size	Parameter	Index of CNFET				
		T_1	T_2	T_3	T_4	T_5
16 nm	D_{cnt}	1.5 nm	1.5 nm	2.4 nm	2.4 nm	4.3 nm
22 nm	D_{cnt}	1.5 nm	1.5 nm	2.3 nm	2.3 nm	3.1 nm
45 nm	D_{cnt}	1.2 nm	1.2 nm	1.5 nm	1.5 nm	2.4 nm

Table 3 Aspect ratio (W/L) of the used MOSFET switches.

Feature size	Index of MOSFET				
	M_1	M_2	M_3	M_4	M_5
16 nm	7.125	4.06	23.75	13.87	23.75
22 nm	7.27	4.09	21.36	14.54	27.72
45 nm	3.7	2.88	14.44	9.33	14.44

Performance evaluation of the FPGA switches

In this sub-section, the power, delay and Power Delay Product (PDP) [29] of the presented CNFET switches are reported. In addition, they are tested extensively in the presence of process and temperature variations to evaluate their immunity against variability for using in FPGAs. Table 4 shows the performance comparison between the CMOS and CNFET switches. According to the results, the PDP of the CNFET switches are considerably lower than the CMOS switches.

Systematic and random process variations are the significant challenges in design of nanoscale devices and circuits. As the feature size of the devices scales down into the nanoranges, the process variations become more critical and degrade the robustness and the performance of the circuits. As a result, some simulations are carried out to evaluate and compare the delay, power consumption and PDP of the MOSFET and CNFET switches in the presence of process variations (i.e. deviations in threshold voltage and the channel length). These variations have considerable impacts on the performance of the nanoscale circuits. Hereupon, Monte Carlo transient analysis is performed using the HSPICE circuit simulator. Distribution of the diameter and channel length is assumed as Gaussian with 3-sigma distribution.

Table 4 Delay, power and PDP of the MOSFET and CNFET switches.

Feature size	Switch type	CMOS			CNFET			PDP improvement (%)
		Delay (ps)	Power (μW)	PDP (aJ)	Delay (ps)	Power (μW)	PDP (aJ)	
45 nm	Switch1 (PT)	12.46	0.08	1.00	0.85	0.02	0.14	85.25
	Buffer	15.89	0.76	12.07	6.81	0.37	2.54	78.89
	Switch2 (TB)	24.81	1.14	28.33	7.51	0.42	3.21	88.66
22 nm	Switch1 (PT)	8.39	0.05	0.45	0.77	0.01	0.005	98.68
	Buffer	8.86	0.72	6.39	3.66	0.34	1.23	80.64
	Switch2 (TB)	13.59	0.91	12.37	3.86	0.36	13.94	88.74
16 nm	Switch1 (PT)	4.58	0.04	0.17	0.67	0.002	0.001	99.07
	Buffer	6.43	1.88	12.12	3.64	0.14	0.53	95.63
	Switch2 (TB)	11.01	2.00	22.03	4.06	0.64	2.6238	88.09
Average improvement (%)								89.29

Figure 4 demonstrates the maximum variations of the delay, power consumption and PDP of the CMOS and CNFET switches at 45 nm, 22 nm and 16 nm feature sizes, with respect to the threshold voltage variations. It can be inferred from the results that the performance of the CNFET-based FPGA switches is less sensitive to the threshold voltage variations, compared to the MOSFET-based FPGA switches, specifically for the smaller feature sizes and larger deviations.

Figure 5 shows the variations of the PDP of the FPGA switches versus channel length variations at 45 nm, 22 nm and 16 nm technology nodes. According to the figure, the CNFET-based FPGA switches experience less parametric variations when the channel lengths of the transistors have variations in comparison with the MOSFET-based FPGA switches and the improvements are more considerable for the smaller feature sizes.

Another important characteristic of the FPGA switches which should be taken into account is their immunity to the ambient temperature variations. We simulated the FPGA switches in a vast range of temperatures (0℃ up to 80℃) to examine their sensitivity to the temperature variations. The power- delay products of the FPGA switches at 16 nm, 22 nm and 45 nm feature sizes are plotted in Figs. 6(a)∼6(c), respectively. It can be inferred from the figure that the CNFET-based FPGA switches are less-sensitive to temperature variation rather than MOSFET-based switches, due to the high thermal stability of CNFETs.

Performance evaluation of CNFET-based FPGAs

The critical path delay and the average power consumption of each FPGA are evaluated at the maximum possible operating frequency of that FPGA using PowerModel and the results are given in Tables 5 and 6,

Table 5 Critical Path Delay ($\times 10^{-8}$ sec).

Benchmark	16 nm			22 nm			45 nm		
	CMOS	CNFET	DI (%)	CMOS	CNFET	DI (%)	CMOS	CNFET	DI (%)
alu4	9.03	7.54	16.50	9.88	7.96	19.4	13.3	7.48	43.9
apex2	8.74	8.97	−2.63	12.0	9.48	21.1	15.1	8.46	44.1
apex4	8.12	7.62	6.16	9.45	7.60	19.5	10.6	12.0	−12.7
bigkey	6.15	4.07	33.8	6.53	3.64	44.3	7.07	5.28	25.3
des	12.6	6.02	52.2	14.0	6.71	52.2	8.79	8.32	5.33
dsip	10.8	5.20	51.8	11.7	3.57	69.6	6.62	4.94	25.3
elliptic	18.2	13.4	26.4	17.8	14.6	18.3	19.7	12.5	36.7
ex5p	11.0	9.10	17.3	9.56	7.65	20.0	11.8	6.74	43.1
ex1010	33.5	14.3	57.3	18.3	19.1	−4.33	46.8	15.5	66.8
frisc	19.4	11.3	41.7	25.2	15.0	40.4	18.6	16.3	12.5
pdc	37.9	25.1	33.7	28.8	19.6	31.9	43.7	26.8	38.7
s298	17.2	17.4	−1.16	17.6	21.6	−22.7	22.1	18.8	15.1
seq	18.8	7.16	61.9	14.7	9.00	38.8	15.2	9.64	36.4
tseng	6.42	4.69	26.9	7.92	5.65	28.7	7.77	5.62	27.6
	Average improvement		30.1%	Average improvement		26.8%	Average improvement		29.3%

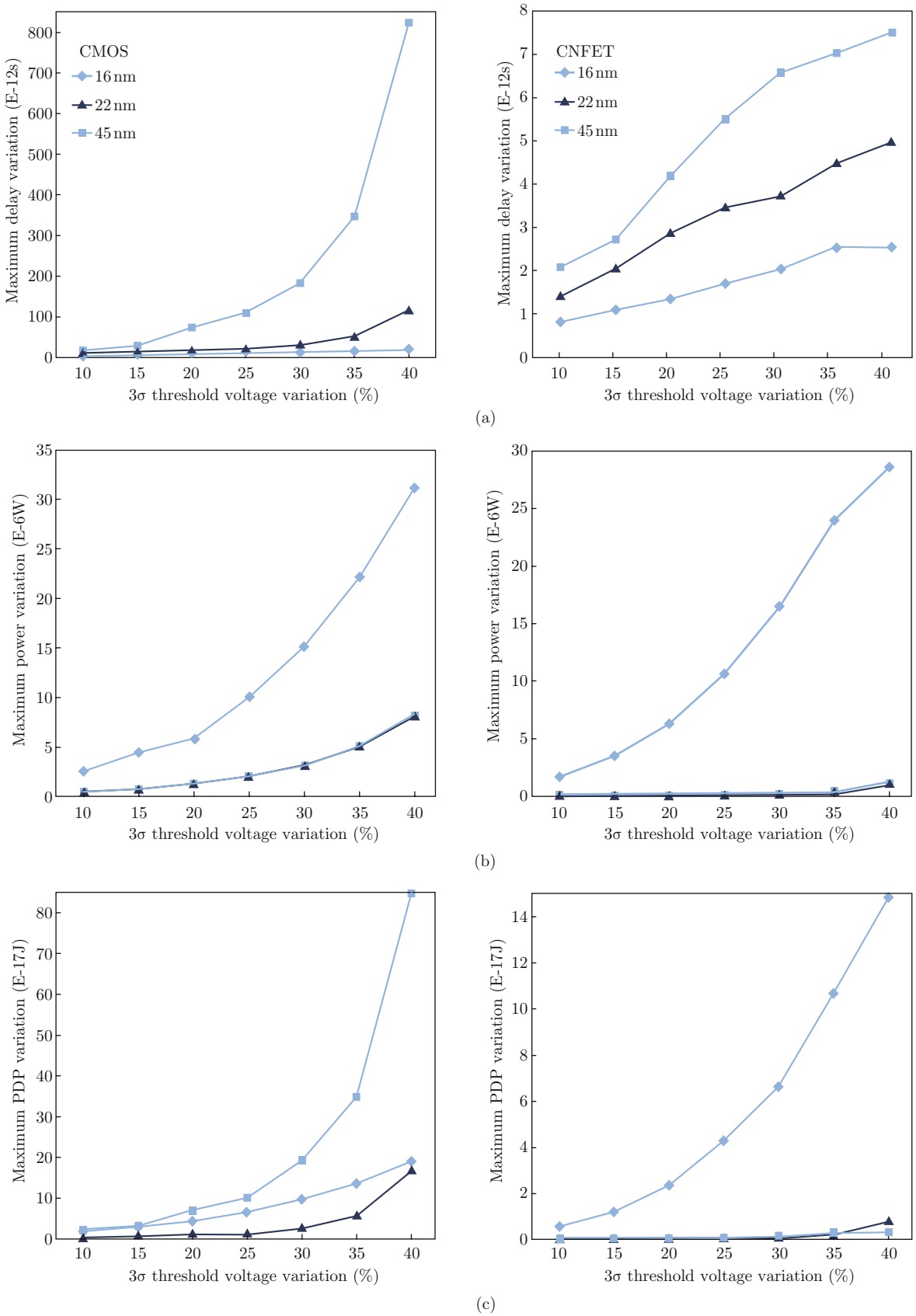

Fig. 4 (a) Delay variation; (b) Power consumption variation; and (c) PDP variation of the FPGA switches with respect to threshold voltage variation.

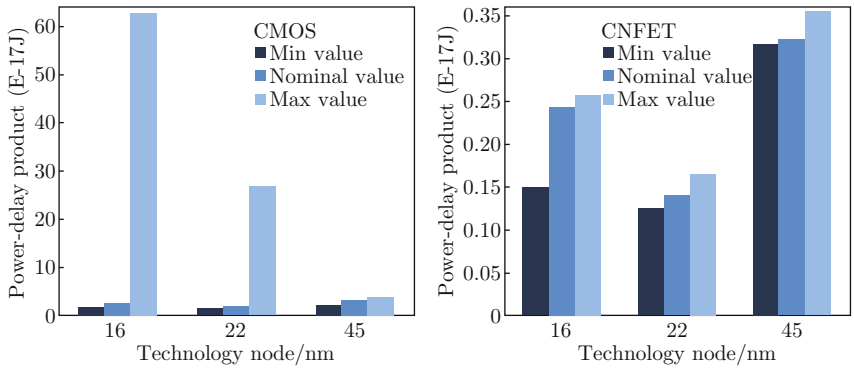

Fig. 5 PDP variation of the FPGA switches versus channel length variations.

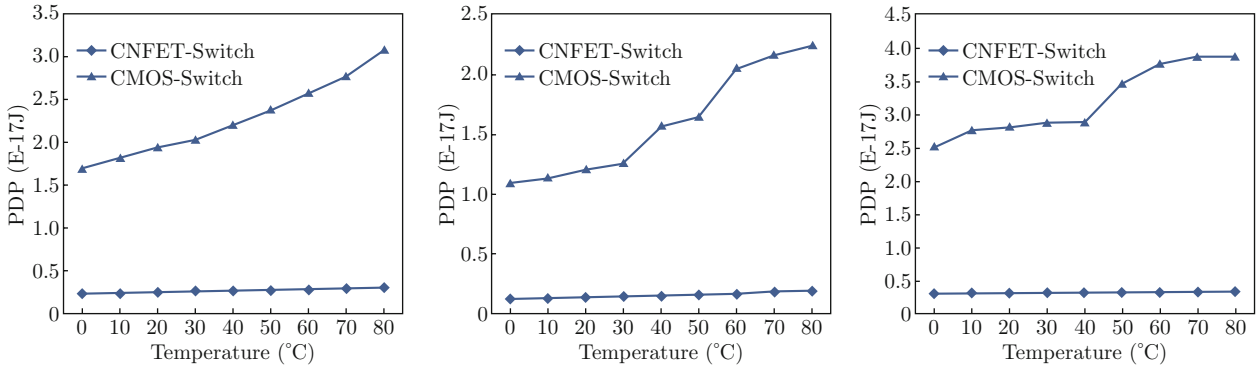

Fig. 6 PDP of the FPGA switches with respect to ambient temperature variations.

Table 6 Average Power Consumption (W).

Benchmark	16 nm			22 nm			45 nm		
	CMOS	CNFET	PI (%)	CMOS	CNFET	PI (%)	CMOS	CNFET	PI (%)
alu4	0.0109	0.0103	5.5046	0.0099	0.0096	3.0303	0.0073	0.0072	1.3698
apex2	0.0145	0.0136	6.2069	0.0105	0.0099	5.7143	0.0081	0.0078	3.7037
apex4	0.0069	0.0065	5.7971	0.0061	0.0056	8.1967	0.0051	0.0051	1.9231
bigkey	0.0227	0.0217	4.4053	0.0211	0.0207	1.8957	0.0197	0.0190	3.5533
des	0.0139	0.0135	2.8777	0.0123	0.0120	2.4390	0.0198	0.0193	2.5252
dsip	0.0115	0.0109	5.2174	0.0106	0.0101	4.7169	0.0187	0.0181	3.2086
elliptic	0.0111	0.0101	9.0090	0.0109	0.0102	6.4220	0.0096	0.0091	5.2083
ex5p	0.0054	0.0050	7.4074	0.0061	0.0057	6.5573	0.0048	0.0047	2.0833
ex1010	0.0059	0.0048	18.644	0.0097	0.0088	9.2783	0.0035	0.0034	2.8571
frisc	0.0064	0.0055	14.062	0.0049	0.0042	14.286	0.0060	0.0058	3.3333
pdc	0.0061	0.0046	24.590	0.0073	0.0059	19.178	0.0041	0.0040	2.4390
s298	0.0075	0.0071	5.3333	0.0074	0.0069	6.7567	0.0057	0.0056	1.7544
seq	0.0061	0.0057	6.5574	0.0075	0.0071	5.3333	0.0072	0.0071	1.3889
tseng	0.0080	0.0078	2.5000	0.0064	0.0061	4.6875	0.0066	0.0064	3.0303
	Average improvement		8.89%	Average improvement		7.21%	Average improvement		2.72%

respectively. In these tables, columns *CMOS* and *CNFET* show the critical path delay or the average total power consumption of the attempted benchmarks with CMOS-based and CNFET-based switches, respectively and the columns *DI* and *PI* represents the improvement of the worst-case delay and the average power consumption of the CNTFET-based FPGAs compared to the MOSFET-based FPGAs, respectively. According to the results of Table 5 and Table 6 using the CNFET-based switches leads to shorter delays, specifically for larger FPGAs and smaller feature sizes and results in almost 30% improvement in terms of critical path delay on average. In addition, it leads to reduction of the power consumption of the FPGAs, specifically at

smaller technology nodes.

In order to make a compromise between the delay and the power consumption of the circuits, the power-delay product (PDP) metric is also calculated. The PDP of the FPGAs at 45 nm, 22 nm and 16 nm technology nodes are plotted in Fig. 7. According to the results, the average of power-delay product in CNFET-based FPGAs are lower than MOSFET-based FPGAs by about 31%, 32% and 36%, at 45 nm, 22 nm and 16 nm feature sizes, respectively. It is worth mentioning that improvement of the PDP of the FPGAs becomes more, when the size of the FPGAs grows and the feature size decreases.

Evaluation of the leakage power dissipation

Leakage power dissipation in nano-regimes is becoming a significant contributor to the power consumption of the CMOS circuits as the channel length, threshold voltage and gate oxide thickness are reduced. Therefore, feasible alternative nanotechnologies such as CNFETs could contribute to reduce the leakage power dissipation, significantly. Therefore, leakage power dissipations are measured in addition to the total power consumption for the FPGAs with CMOS-based and CNFET-based switches. The result of this experiment is shown in Table 7 for 45 nm, 22 nm and 16 nm feature sizes. In this table, column *LI* represents the leakage power improvement of CNFET switches compared to the MOS switches. It can be inferred from the results that utilizing the CNFET-based FPGA switches leads to extremely significant reduction of the leakage power dissipation of the FPGAs.

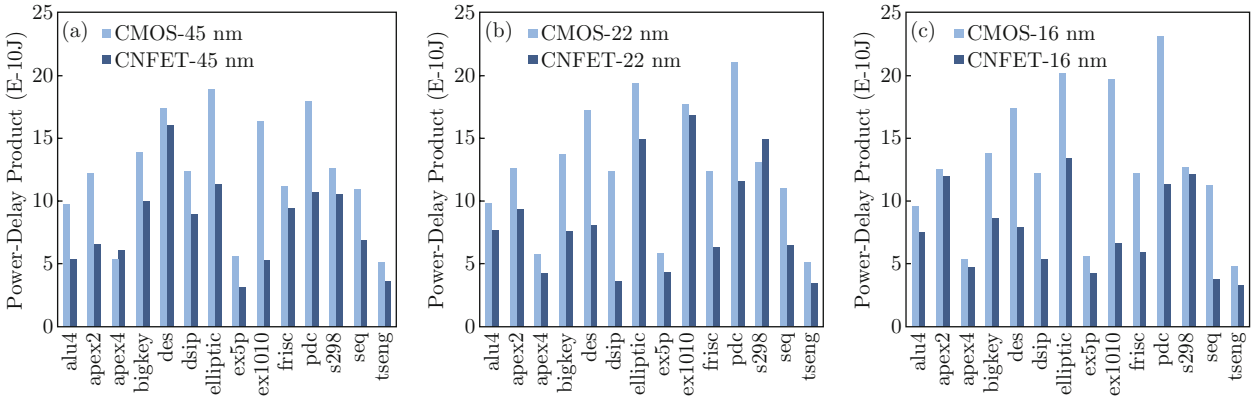

Fig. 7 PDP of FPGAs (a) At 45 nm; (b) At 22nm; and (c) At 16 nm.

Table 7 Leakage Power Dissipation (W).

Benchmark	16 nm			22 nm			45 nm		
	CMOS	CNFET	LI (%)	CMOS	CNFET	LI (%)	CMOS	CNFET	LI (%)
alu4	3.29E-4	6.98E-06	97.88	2.28E-4	9.41E-07	99.58	1.85E-05	4.50E-08	99.7572
apex2	4.86E-4	1.01E-05	97.92	3.36E-4	1.33E-06	99.60	2.70E-05	6.21E-08	99.77
apex4	3.62E-4	7.26E-06	97.99	2.44E-4	9.43E-07	99.61	1.91E-05	4.30E-08	99.77
bigkey	3.65E-4	8.34E-06	97.71	2.33E-4	1.13E-06	99.51	2.12E-05	2.12E-05	99.76
des	5.45E-4	1.05E-05	98.06	4.06E-4	1.38E-06	99.65	2.97E-05	5.83E-08	99.80
dsip	2.97E-4	5.95E-06	97.99	2.70E-4	1.05E-06	99.60	2.05E-05	4.80E-08	99.76
elliptic	8.42E-4	1.95E-05	97.68	5.94E-4	2.50E-06	99.57	5.00E-05	1.13E-07	99.77
ex5p	2.88E-4	6.05E-06	97.89	1.85E-4	7.74E-07	99.58	1.59E-05	3.64E-08	99.77
ex1010	1.13E-3	2.45E-05	97.83	7.98E-4	7.98E-4	99.60	6.02E-05	1.45E-07	99.75
frisc	8.81E-4	1.91E-05	97.82	6.36E-4	2.53E-06	99.60	4.90E-05	1.14E-07	99.76
pdc	1.54E-3	3.27E-05	97.87	1.11E-3	4.07E-06	99.63	8.48E-05	1.74E-07	99.79
s298	3.52E-4	7.80E-06	97.78	2.50E-4	1.05E-06	99.58	2.18E-05	5.65E-08	99.74
seq	4.29E-4	9.56E-06	97.77	2.97E-4	1.20E-06	99.59	2.39E-05	5.85E-08	99.75
tseng	1.94E-4	4.35E-06	97.75	6.41E-3	5.81E-07	99.99	1.10E-05	2.90E-08	99.73
	Average improvement		97.85%	Average improvement		99.62%	Average improvement		99.76%

Evaluation of the area of the FPGAs

An FPGA is composed of a two-dimensional array of configuration logic blocks and switch boxes. In regular FPGAs, each switch box consists of a crossbar switch structure that enables connecting the vertical and horizontal routing tracks. The organization of segment-to-segment connections inside a switch box is an important factor in routability and performance of an FPGA. Switch block designers typically assumed a FPGA routing structure only contained wire segments which span a single logic block. Therefore, each input track of a switch box can be connected to three other tracks (Fs=3). Disjoint and Wilton, depicted in Fig. 8, are the common switch block structures. As illustrated in Fig. 8, a wire entering a disjoint switch block can only connect to the other wires with the same numerical designation via programmable switches. As a result, potential source-destination routes in the FPGA are isolated into distinct routing domains, limiting routing flexibility. The Wilton switch block uses the same number of routing switches as the disjoint switch block but overcomes the domain issue by allowing for a change in domain assignment on connections that turn. In both structures, the number of switches for 4-channel FPGA is 24.

As mentioned before, there are two types of switches in each switch box, i.e. pass transistors and tri-state buffers. Each pass transistor switch is an N-type transistor and each tri-state buffer switch has 5 transistors. In addition, we assumed that 50% of all switches are buffered which is a normal assumption in a canonical FPGA design. Consequently, the number of transistors used in switch boxes in an FPGA with N rows and N columns is as follows:

$$N_{tr} = 24N^2(0.5 \times 5 + 0.5 \times 1) = 72N^2 \qquad (10)$$

Total estimated area of MOSFET-based FPGA witches and CNFET-based switches are compared in Table 8. As in modern FPGAs, more than 65% of the FPGA area is related to routing switches [1,30], it is

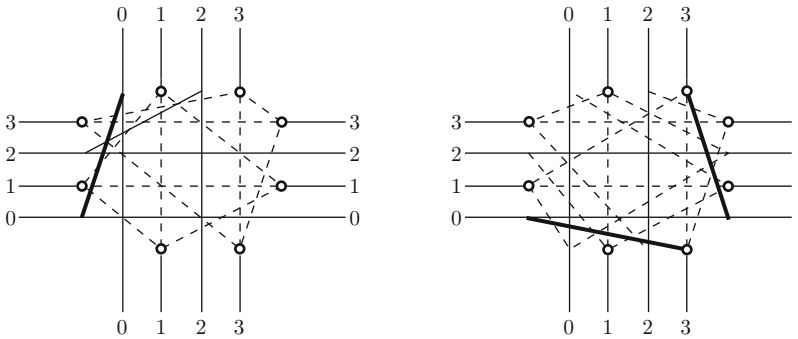

Fig. 8 Switch box styles (a) Disjoint (b) Wilton.

Table 8 Area of the FPGAs (μm^2).

Benchmark	DIM	#Switch	45 nm		22 nm		16nm	
			CMOS	CNFET	CMOS	CNFET	CMOS	CNFET
alu4	20	28800	1308.96	1218.24	627.26	443.52	355.05	267.26
apex2	23	38088	1731.10	1611.12	829.56	586.56	469.55	353.46
apex4	19	25992	1181.34	1099.46	566.11	400.28	320.43	241.21
bigkey	27	52488	2385.58	2220.24	1143.19	808.32	647.07	487.09
des	32	73728	3350.94	3118.69	1605.80	1135.41	908.92	684.20
dsip	27	52488	2385.58	2220.24	1143.19	808.32	647.07	487.09
elliptic	31	69192	3144.78	2926.82	1507.00	1065.56	853.00	642.10
ex5p	17	20808	945.72	880.18	453.20	320.44	256.52	193.10
ex1010	35	88200	4008.69	3730.86	1921.00	1358.28	1087.33	818.50
frisc	30	64800	2945.16	2741.04	1411.34	997.92	798.85	601.34
pdc	35	88200	4008.69	3730.86	1921.00	1358.28	1087.33	818.50
s298	23	38088	1731.10	1611.12	829.56	586.56	469.55	353.46
seq	22	34848	1583.84	1474.07	758.99	536.66	429.61	323.39
tseng	17	20808	945.72	880.18	453.20	320.44	256.52	193.10
Average improvement			6.93%		29.29%		24.72%	

estimated that the average area improvements of the attempted benchmarks at 45 nm, 22 nm and 16 nm is more than 5%, 20% and 17%, respectively. It is worthwhile mentioning that the area improvement is more considerable for the larger FPGAs and at smaller technology nodes.

Conclusion

Routing resources are the major bottleneck in modern FPGAs that affect their performance and power consumption considerably. Utilizing CNFETs has been reported as an effective solution to alleviate the interconnect problems. The results of the simulations, conducted in this paper, demonstrate that the CNFET-based FPGA switches outperform the MOSFET based ones in terms of energy efficiency and insusceptibility to temperature and process variations. In this paper hybrid FPGA architecture is presented which takes advantage of CNFET and MOSFET devices, concurrently. Experimental results show that the performance of CNFET-based FPGAs is improved about 30% and the average power consumption is reduced more than 6% on average. Moreover, it leads to significant reduction of leakage power dissipation and smaller chip area.

References

[1] A. Gayasen, N. Vijaykrishnan and M. J. Irwin, IEEE 42nd annual Design Automation Conference, 921, June (2005).

[2] G. Cho, Y. B. Kim, F. Lombardi and M. Choi, IEEE International Instrumentation and Measurement Technology Conference, 909, May (2009).

[3] M. A. Tehrani, F. Safaei, M. H. Moaiyeri and K. Navi, Microelectron. J. 42, 913 (2011). http://dx.doi.org/10.1016/j.mejo.2011.03.004

[4] M. H. Moaiyeri, R. F. Mirzaee, K. Navi and O. Hashemipour, Nano-Micro Lett. 3, 43 (2011). http://dx.doi.org/10.5101/nml.v3i1.p43-50

[5] M. H. Moaiyeri, A. Doostaregan and K. Navi, IET Circ. Dev. Syst. 5, 285 (2011).

[6] K. Navi, R. Sharifi Rad, M. H. Moaiyeri and A. Momeni, Nano-Micro Lett. 2, 114 (2010). http://dx.doi.org/10.5101/nml.v2i2.p114-120

[7] L. K. Scheffer, IEEE 44th annual Design Automation Conference, 576, June (2007).

[8] N. Patil, A. Lin, J. Zhang, H. P. Wong, and S. Mitra, IEEE 46th Annual Design Automation Conference, 304, July (2009).

[9] G. F. Close and H. P. Wong, IEEE Trans. Nanotech. 7, 596 (2008). http://dx.doi.org/10.1109/TNANO.2008.927373

[10] C. Dong, S. Chilstedt and D. Chen, ACM/SIGDA 17th International Symposium on Field Programmable Gate Arrays, 161, Feb. (2009).

[11] S. Eachempati, A. Nieuwoudt, A. Gayasen, N. Vijaykrishnan and Y. Massoud, IEEE conference on Design, automation and test in Europe, 1, April 2007.

[12] W. Zhang, N. K. Jha, and L. Shang, IEEE 43rd Annual Design Automation Conference, 711, July 2006.

[13] M. Jamalizadeh, F. Sharifi, M. H. Moaiyeri, K. Navi and O. Hashemipour, Nano-Micro Lett. 2, 227 (2010).

[14] K. Natori, Y. Kimura and T. Shimizu, J. Appl. Phys. 97, 034306 (2005). http://dx.doi.org/10.1063/1.1840096

[15] Y. B. Kim, Y. B. Kim and F. Lombardi, IEEE International Midwest Symposium on Circuits and Systems, 1130, August 2009.

[16] J. Deng, "Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors", Doctoral Dissertation, Stanford University, 2007.

[17] J. Deng and H. P. Wong, IEEE Trans. Electron Dev. 54, 3186 (2007). http://dx.doi.org/10.1109/TED.2007.909030

[18] M. S. Haque, K. B. K. Teo, N. L. Rupensinghe, S. Z. Ali, I. Haneef, S. Maeng, J. Park, F. Udrea and W. I. Milne, Nanotechnology 19, 025607 (2008). http://dx.doi.org/10.1088/0957-4484/19/02/025607

[19] G. F. Close, S. Yasuda, B. Paul, S. Fujita and H. P. Wong, Nano Lett. 8, 706 (2008). http://dx.doi.org/10.1021/nl0730965

[20] K. Siozios, D. Soudris and G. Economakos, IEEE 16th International conference on Digital Signal Processing, 1, July 2009.

[21] A. Raychowdhury and K. Roy, IEEE T. Circuits Syst. 54, 2391 (2007). http://dx.doi.org/10.1109/TCSI.2007.907799

[22] A. Javey, J. Guo, D. Farmer, Q. Wang, E. Yenilmez, R. Gordon, M. Lundstrom and H. Dai, Nano Lett. 4, 1319 (2004). http://dx.doi.org/10.1021/nl049222b

[23] A. Javey, R. Tu, D. B. Farmer, J. Guo, R. G. Gordon and H. Dai, Nano Lett. 5, 345 (2005). http://dx.doi.org/10.1021/nl047931j

[24] S. O. Koswatta, D. E. Nikonov and M. S. Lundstrom, IEEE 27th Proceedings of the Technology Digest International Electron Device Meeting, 518, December 2005.

[25] X. Li, H. Yang and H. Zhong, IEEE 8th International Conference on Solid-State and Integrated Circuit Technology, 1880, October 2006.

[26] K. K. W. Poone, S. J. E. Wilton and A. Yan, ACM Transactions on Design Automation of Electronic Systems 10, 187 (2005).

[27] BLAC CAD Group, MCNC benchmarks, Available on http://vlsicad.cs.binghamton.edu/benchmarks.html, 2010.

[28] J. Deng and H. P. Wong, IEEE T. Electron. Dev. 54, 3195 (2007). http://dx.doi.org/10.1109/TED.2007.909043

[29] M. H. Moaiyeri, R. F. Mirzaee, K. Navi, T. Nikoubin and O. Kavehei, Int. J. Electro. 97, 647 (2010). http://dx.doi.org/10.1080/00207211003646944

[30] I. Kuon, R. Tessier and J. Rose, Foundations and Trends in Electronic Design Automation, 2, 135 (2007). http://dx.doi.org/10.1561/1000000005